SAMSUNG

TDMA MOBILE TELEPHONE

STH-N375

SERVICE *Manual*

TDMA MOBILE TELEPHONE

CONTENTS

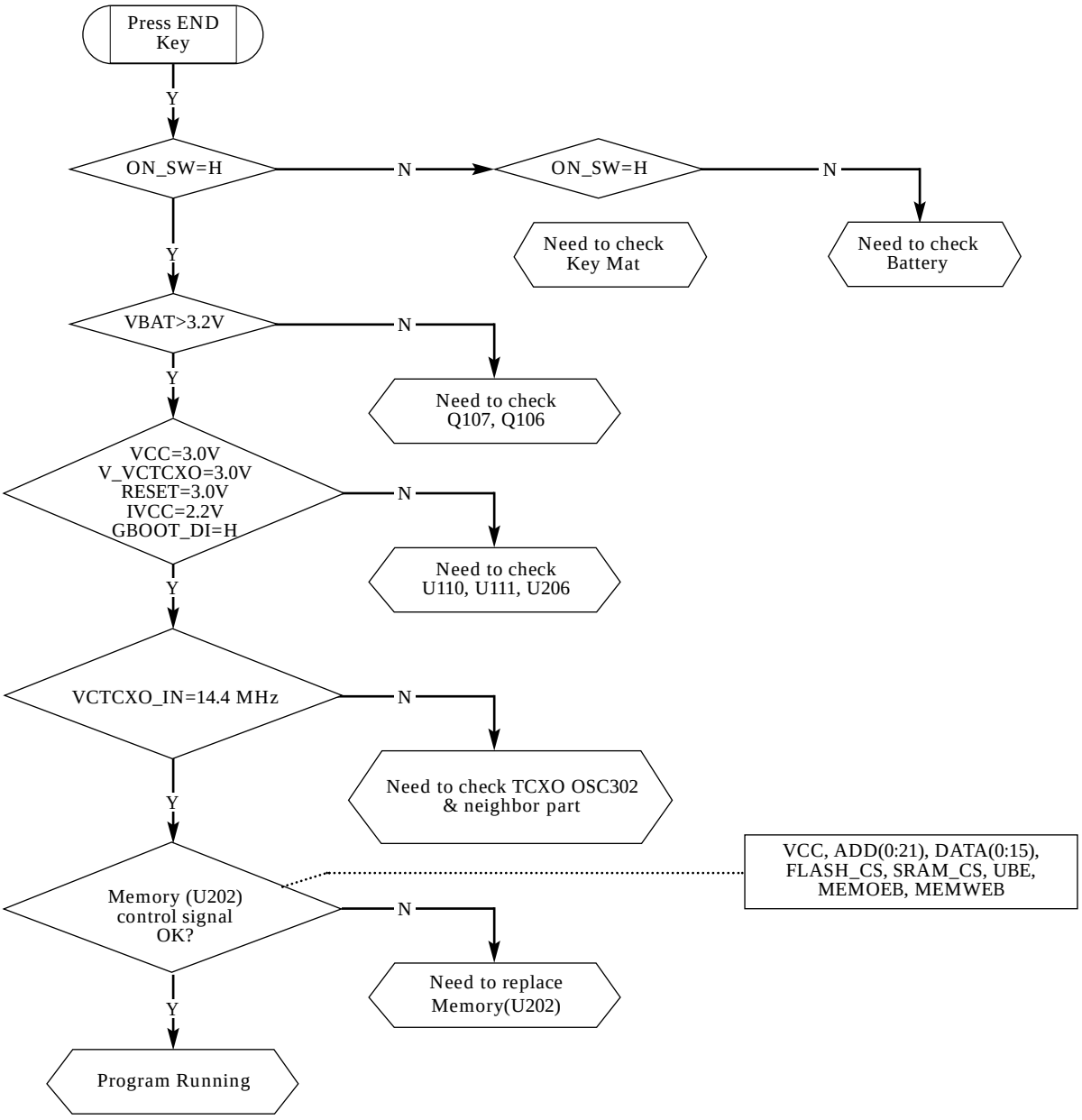
ELECTRONICS

Printed in Korea.
Code No.: GH68-02790A
BASIC.

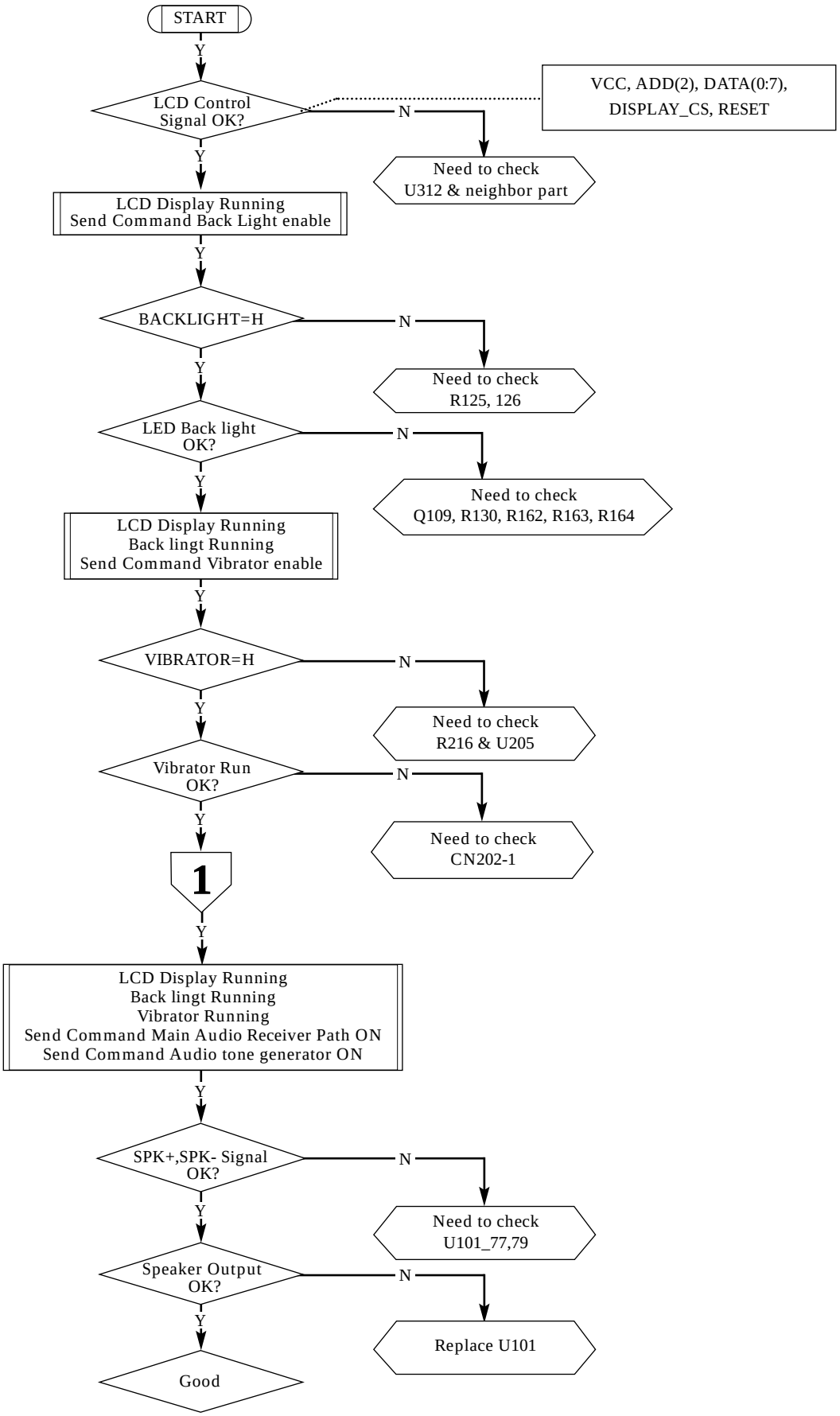
1. STH-N375 Trouble Shooting

1. Baseband Section

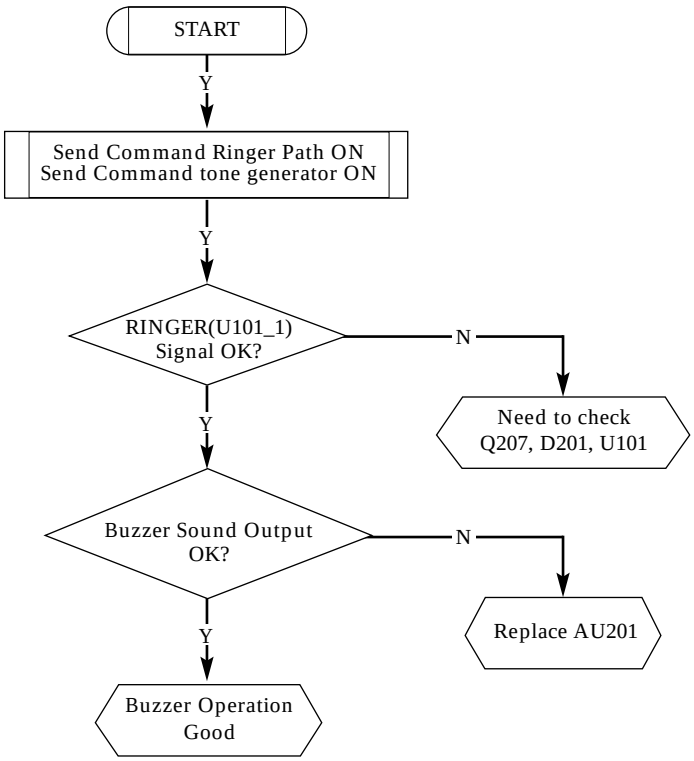
1-1. Program No Running



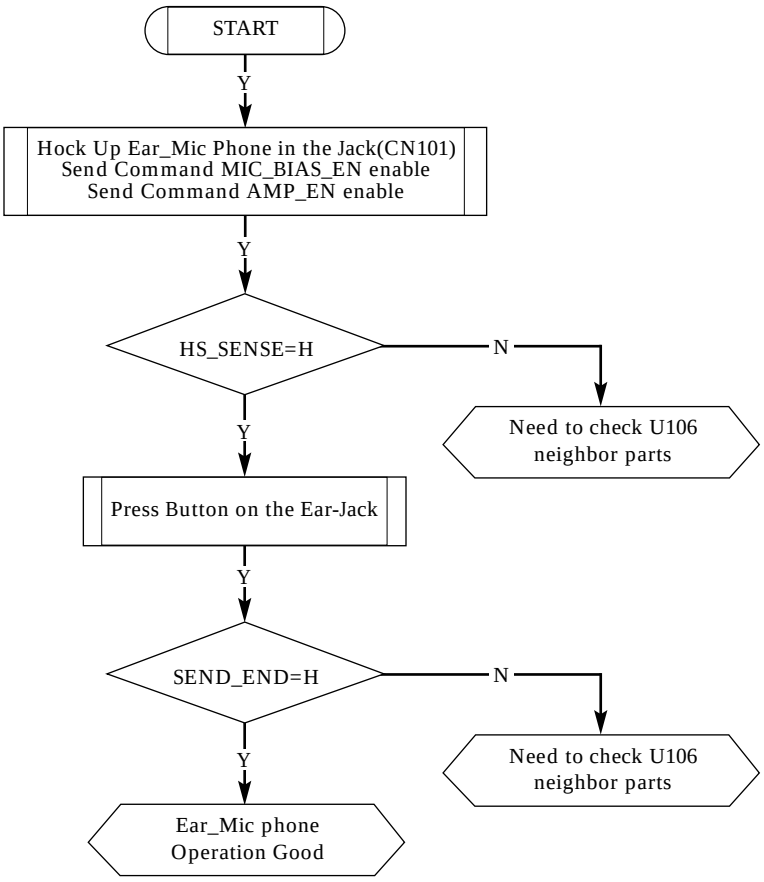
1-2. Abnormal LCD Module, Vibrator & Speaker Operation



1-3. Abnormal Buzzer operation

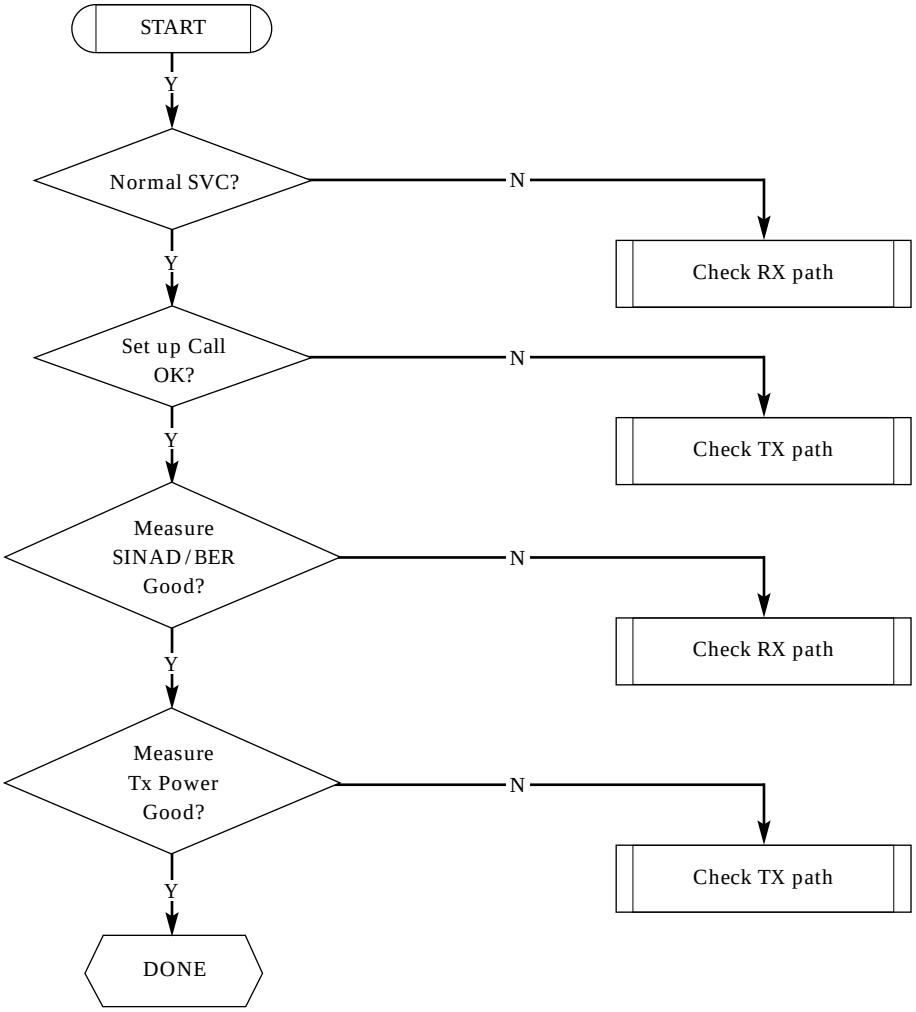


1-4. Abnormal external Ear_Mic Jack operation

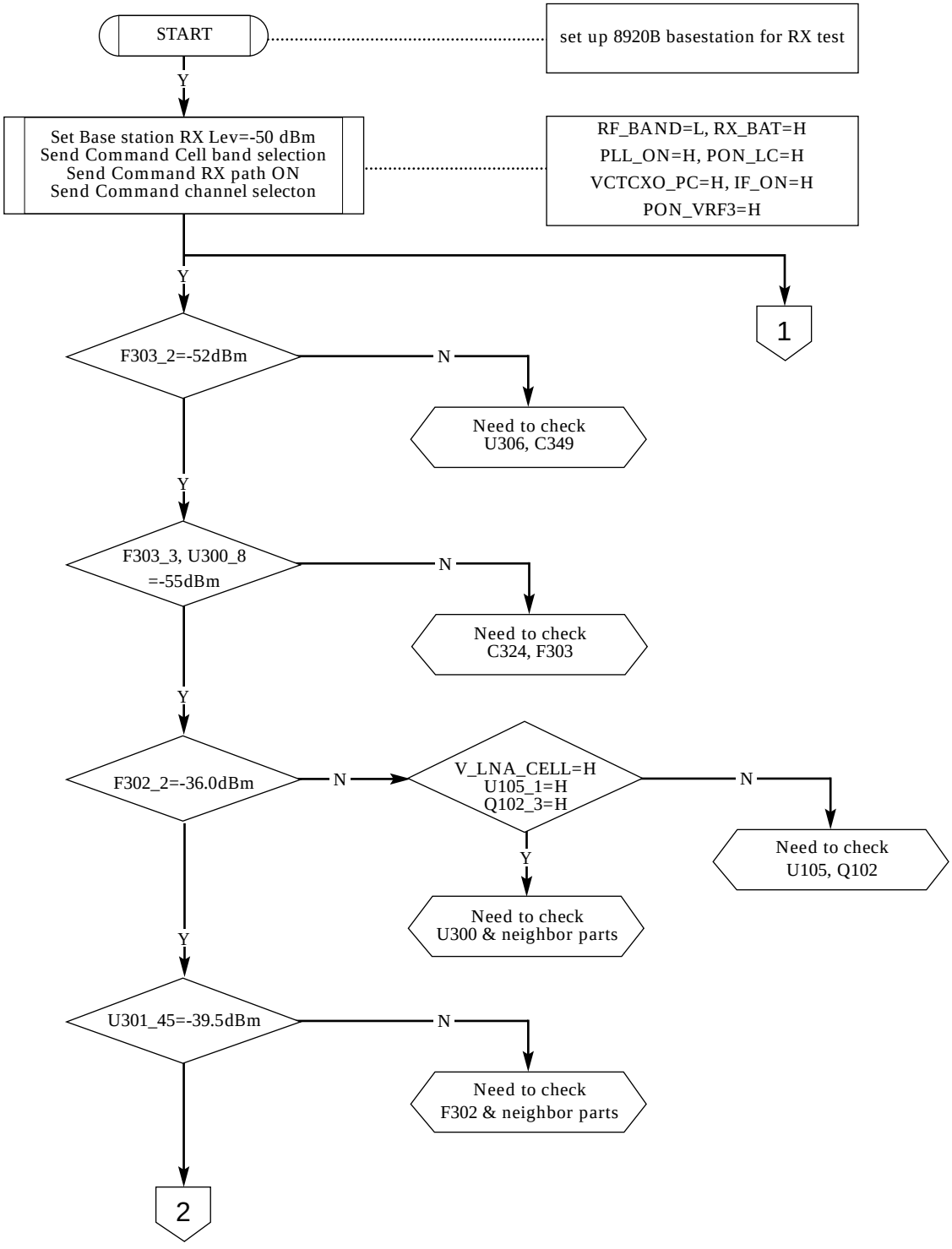


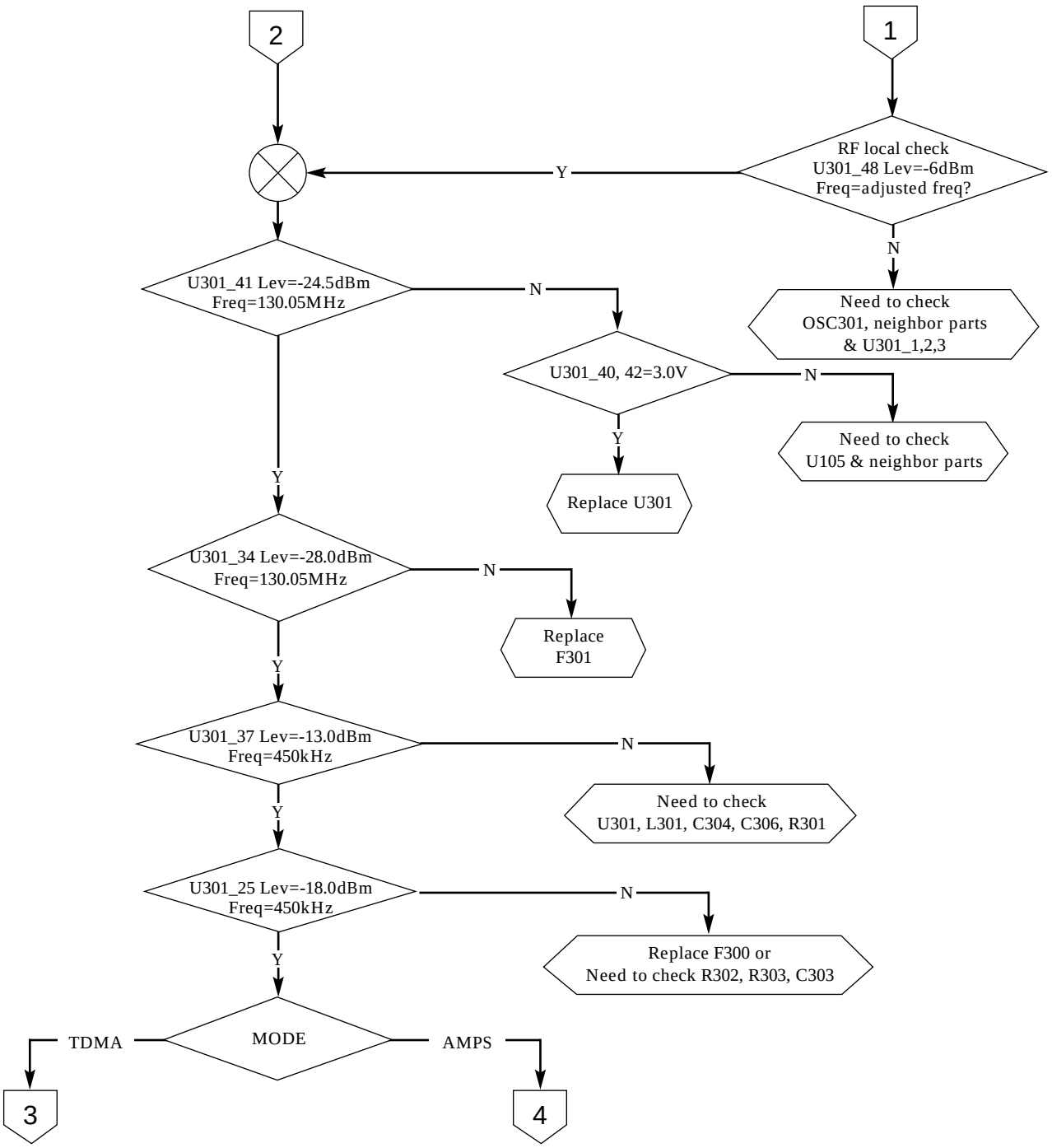
2. RF Section

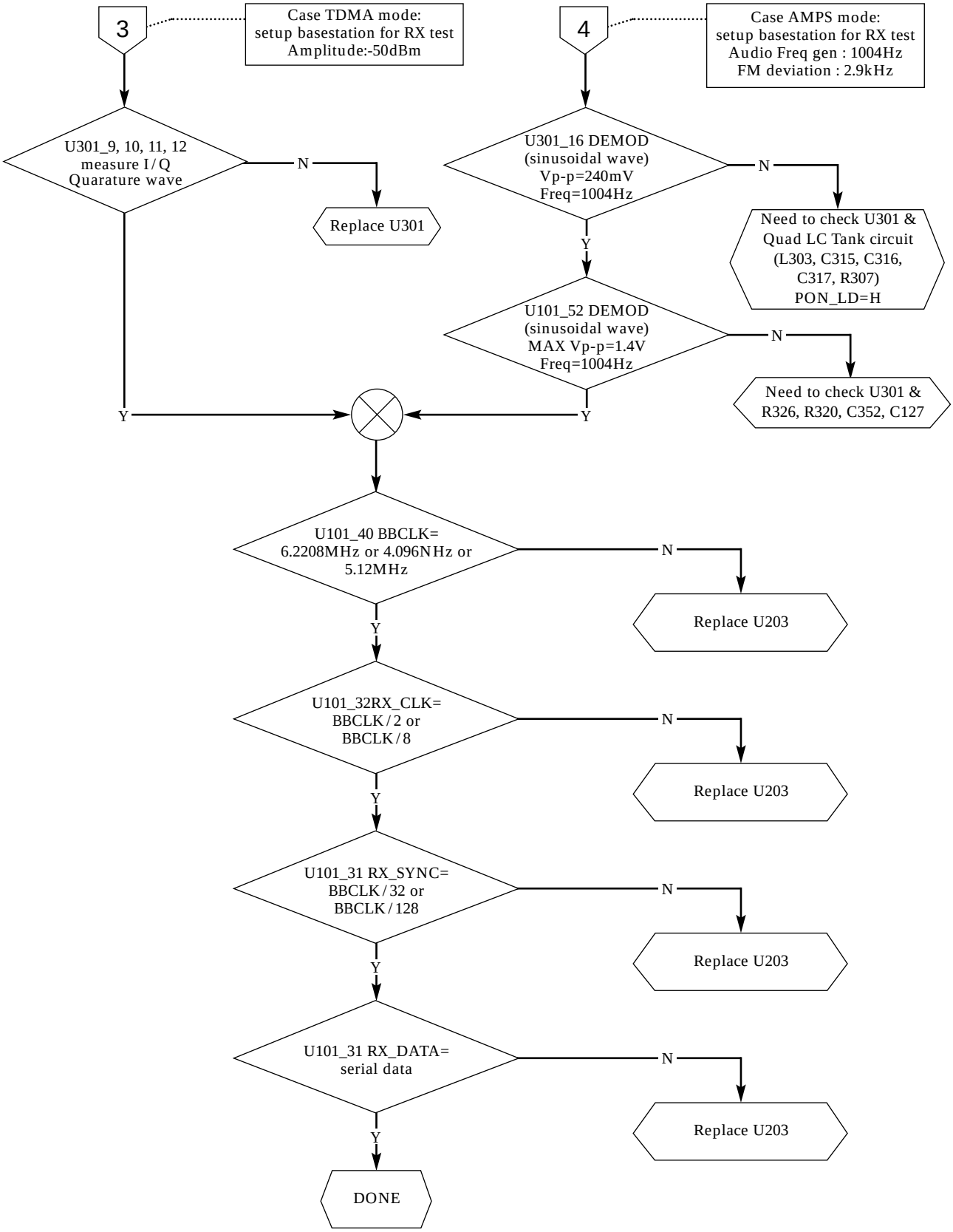
2-1. Call processing and Online Test



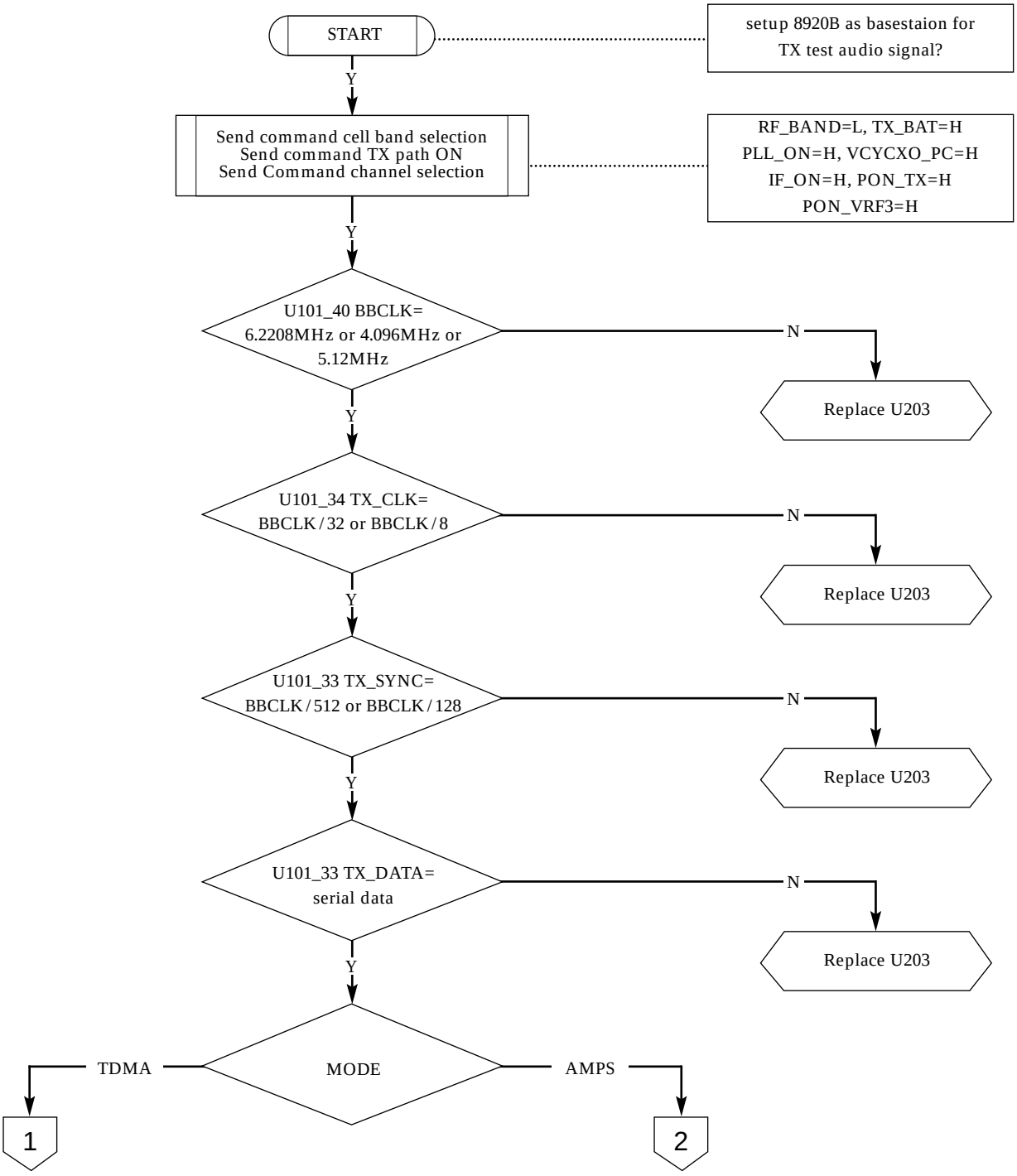
2-2. Receiver Section (Offline test)

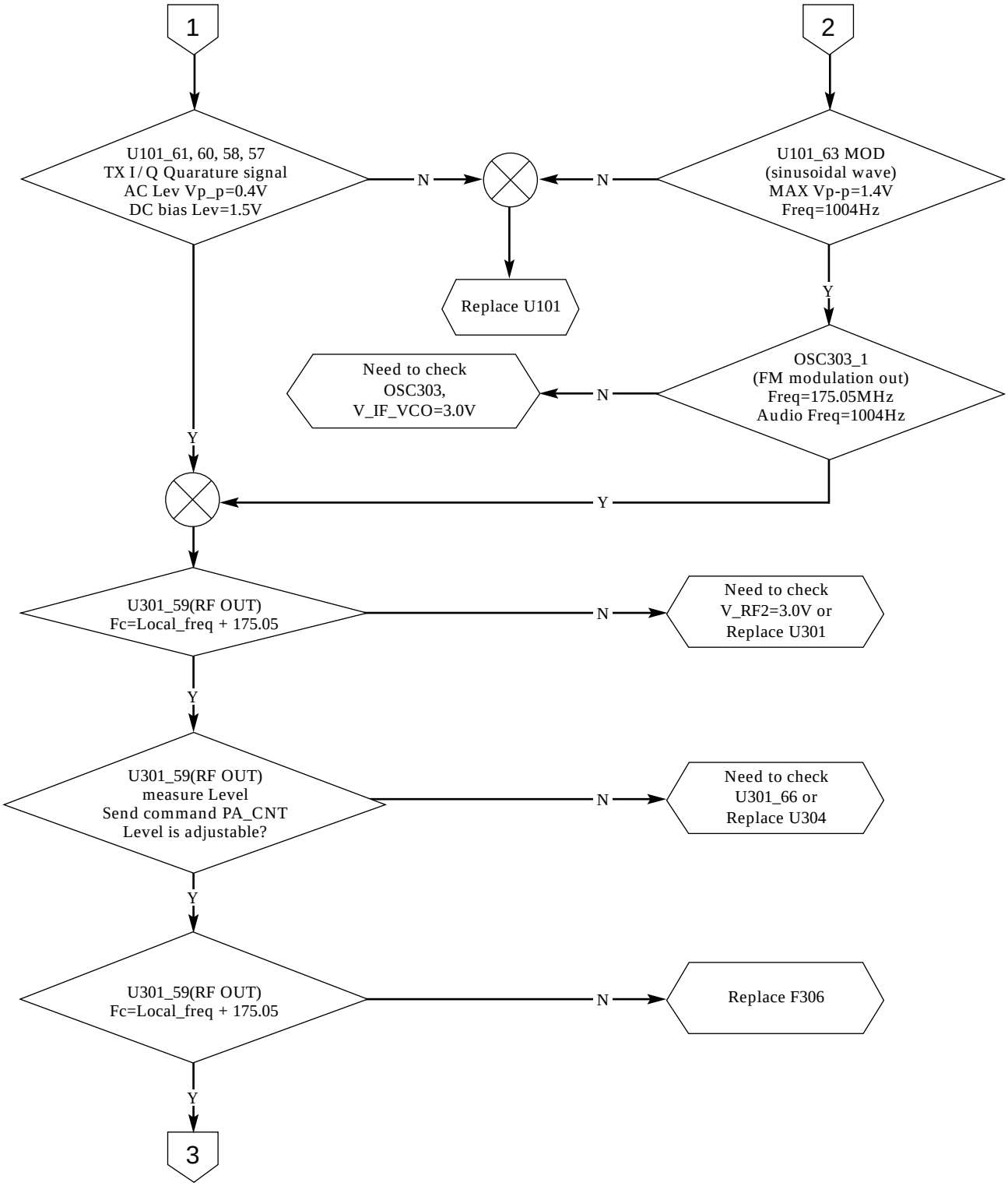


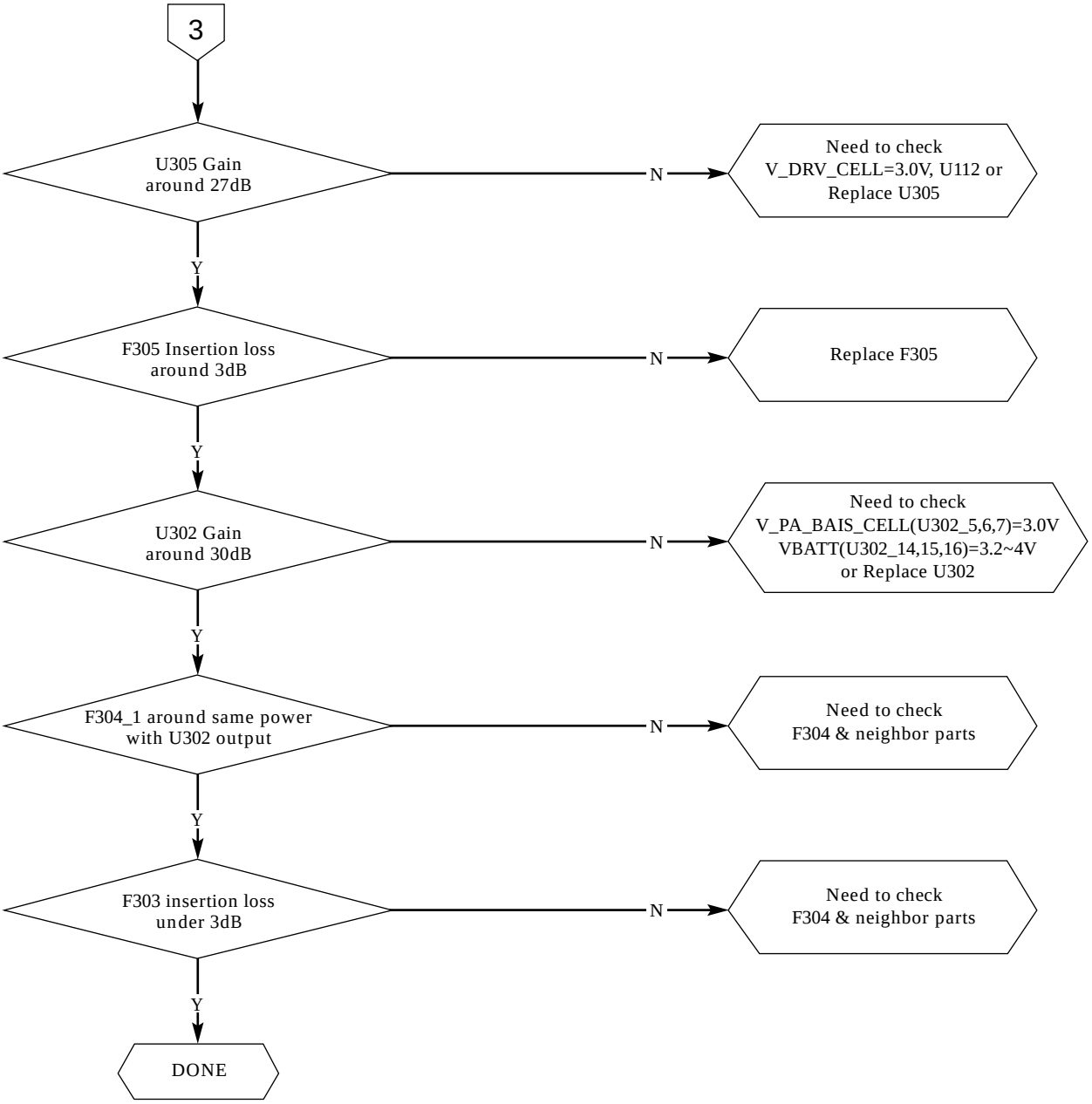

2
1
RF local check
U301_48 Lev=-6dBm
Freq=adjusted freq?
Y
N
U301_41 Lev=-24.5dBm
Freq=130.05MHz
N
Need to check
OSC301, neighbor parts
& U301_1,2,3
U301_40, 42=3.0V
N
Y
Need to check
U105 & neighbor parts
Replace U301
Y
U301_34 Lev=-28.0dBm
Freq=130.05MHz
N
Replace
F301
Y
U301_37 Lev=-13.0dBm
Freq=450kHz
N
Need to check
U301, L301, C304, C306, R301
Y
U301_25 Lev=-18.0dBm
Freq=450kHz
N
Replace F300 or
Need to check R302, R303, C303
Y
MODE
TDMA
AMPS
3
4


3
Case TDMA mode:
setup basestation for RX test
Amplitude:-50dBm
4
Case AMPS mode:
setup basestation for RX test
Audio Freq gen : 1004Hz
FM deviation : 2.9kHz
U301_9, 10, 11, 12
measure I/Q
Quarature wave
N
Replace U301
Y
U301_16 DEMOD
(sinusoidal wave)
Vp-p=240mV
Freq=1004Hz
N
Need to check U301 &
Quad LC Tank circuit
(L303, C315, C316,
C317, R307)
PON_LD=H
Y
U101_52 DEMOD
(sinusoidal wave)
MAX Vp-p=1.4V
Freq=1004Hz
N
Need to check U301 &
R326, R320, C352, C127
Y
Y
U101_40 BBCLK=
6.2208MHz or 4.096NHz or
5.12MHz
N
Replace U203
Y
U101_32RX_CLK=
BBCLK/2 or
BBCLK/8
N
Replace U203
Y
U101_31 RX_SYNC=
BBCLK/32 or
BBCLK/128
N
Replace U203
Y
U101_31 RX_DATA=
serial data
N
Replace U203
Y
DONE

2-3.Transmitter Section (Offline test)

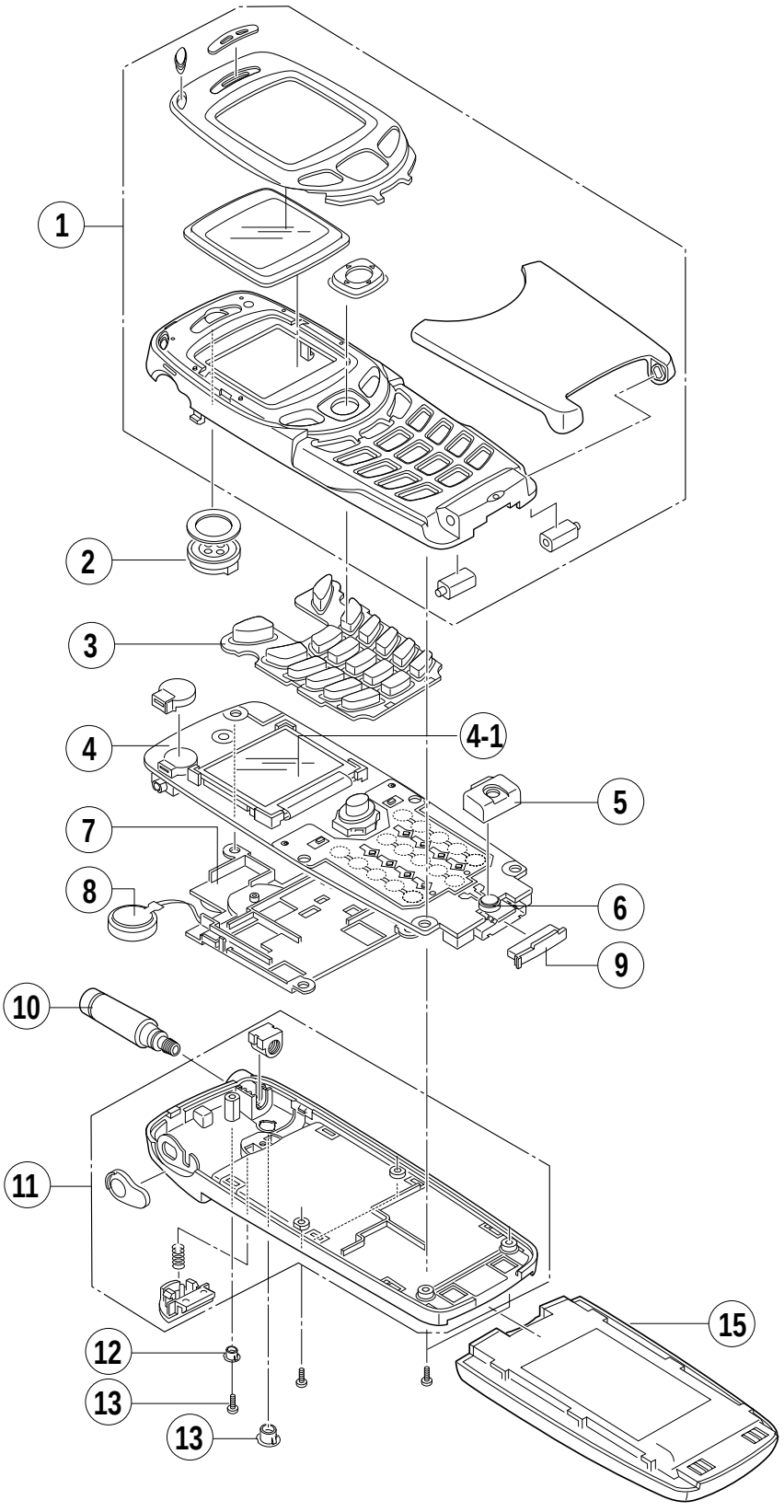



1
2
U101_61, 60, 58, 57
TX I/Q Quarature signal
AC Lev Vp_p=0.4V
DC bias Lev=1.5V
N
N
U101_63 MOD
(sinusoidal wave)
MAX Vp-p=1.4V
Freq=1004Hz
Replace U101
Y
Need to check
OSC303,
V_IF_VCO=3.0V
N
OSC303_1
(FM modulation out)
Freq=175.05MHz
Audio Freq=1004Hz
Y
Y
U301_59(RF OUT)
Fc=Local_freq + 175.05
N
Need to check
V_RF2=3.0V or
Replace U301
Y
U301_59(RF OUT)
measure Level
Send command PA_CNT
Level is adjustable?
N
Need to check
U301_66 or
Replace U304
Y
U301_59(RF OUT)
Fc=Local_freq + 175.05
N
Replace F306
Y
3


3
U305 Gain
around 27dB
N
Need to check
V_DRV_CELL=3.0V, U112 or
Replace U305
Y
F305 Insertion loss
around 3dB
N
Replace F305
Y
U302 Gain
around 30dB
N
Need to check
V_PA_BAIS_CELL(U302_5,6,7)=3.0V
VBATT(U302_14,15,16)=3.2~4V
or Replace U302
Y
F304_1 around same power
with U302 output
N
Need to check
F304 & neighbor parts
Y
F303 insertion loss
under 3dB
N
Need to check
F304 & neighbor parts
Y
DONE

3. STH-N375 Exploded View and its Parts List

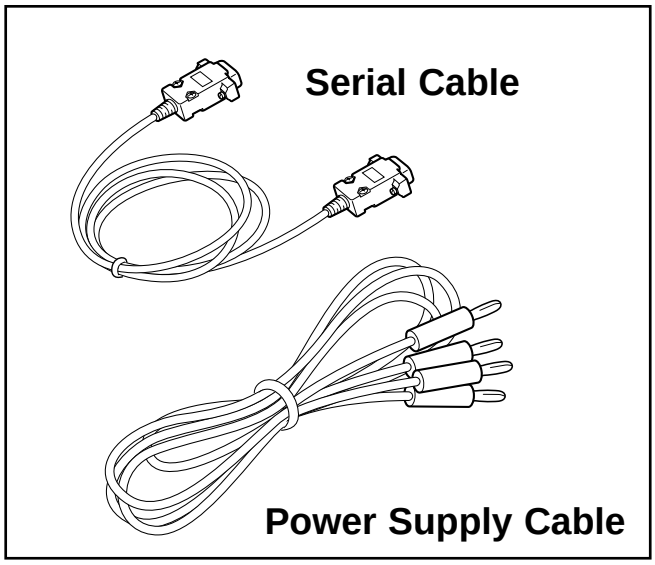
1. Cellular phone Exploded View



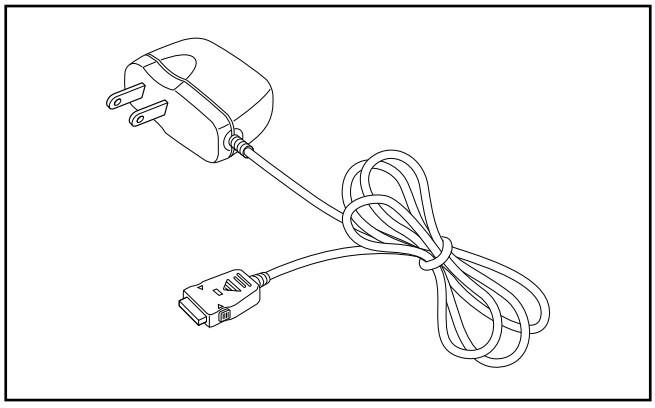
2. Cellular phone Parts List

Location No.		Description	SEC CODE	Remark
			Silver	
1		FRONT COVER	GH75-01724A	
2		SPEAKER	3001-001210	
3		KEY PAD	GH75-01826A	
4		MAIN PBA	GH82-00107A	
	4-1	LCD	GH07-00143A	
5		MIC HOLDER	GH73-01024A	
6		MIC	GH59-00376A	
7		SHIELD COVER	GH75-01895A	
8		VIBRATOR	GH31-00019A	
9		COVER CONNECT	GH73-01026A	
10		ANTENNA	GH42-00141G	
11		REAR COVER	GH72-03845A	
12		SCREW DUMMY	GH73-01130A	
13		SCREW (M1.7 x L3.5)	6001-001319	
14		RF JACK COVER	GH73-01027A	
15		BATTERY	GH43-00490A	900mAh

3. Test Jig (GH80-00614A)



4. TC (GH44-00145G) 110V
Mexico, Colombia, Brazil

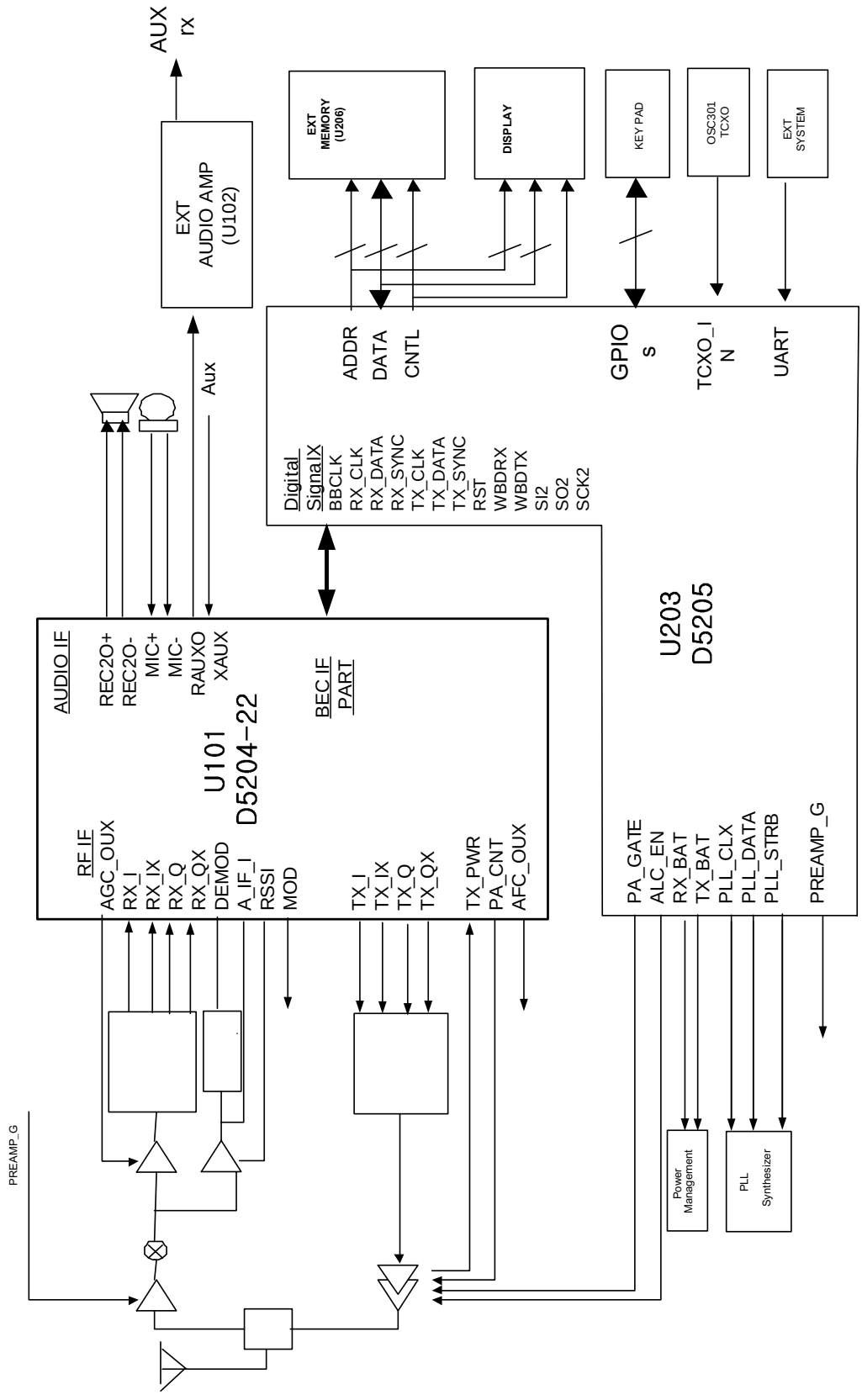


5. RF Test Cable (GH39-00090A)

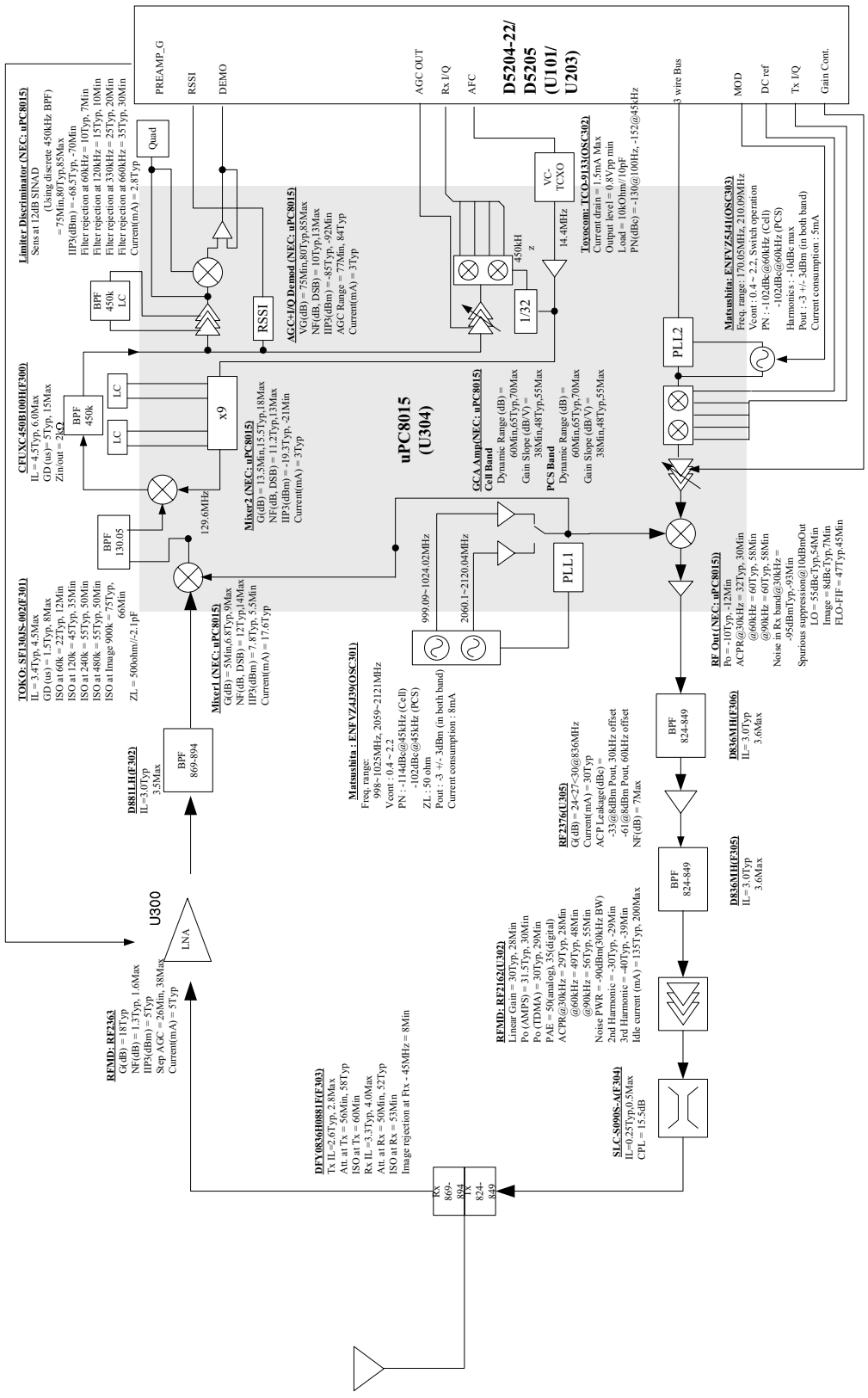
6. Test Cable (GH39-00092A)

4. STH-N375 Block Diagrams

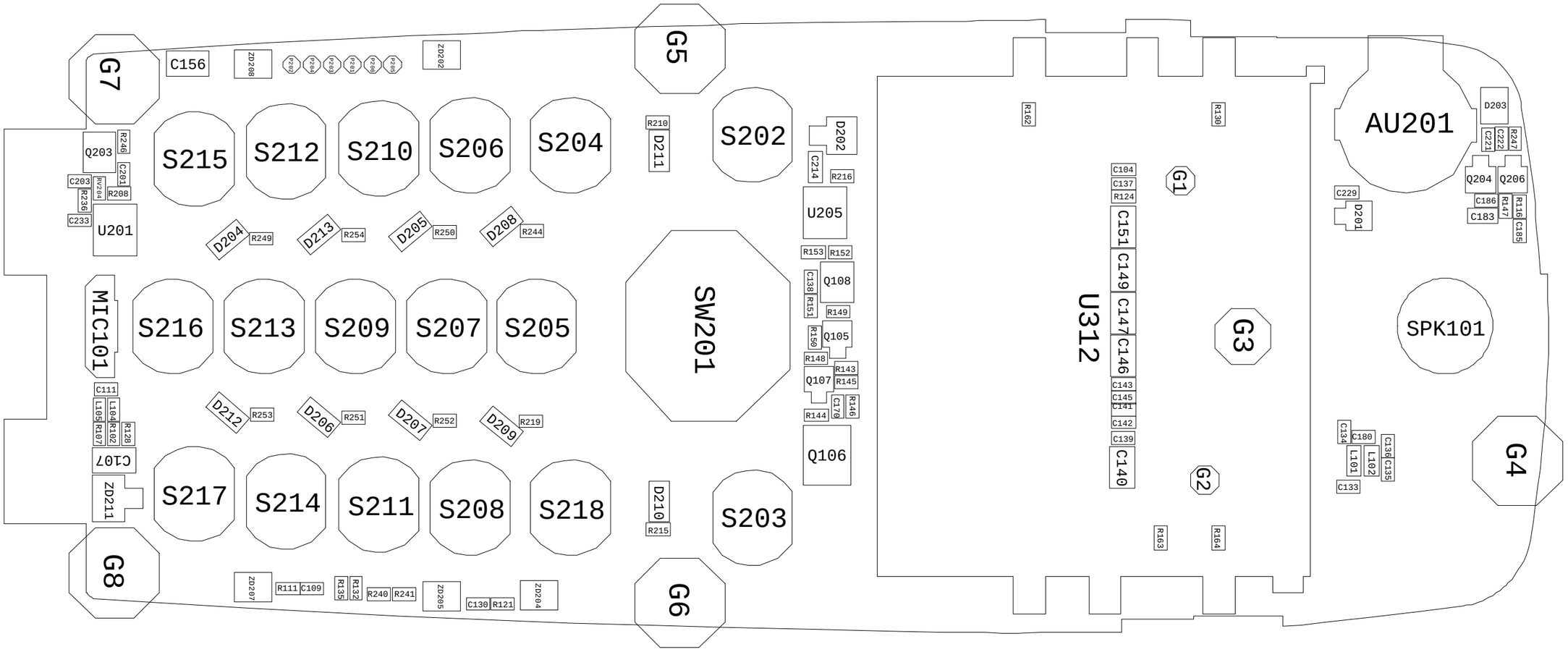
1. Base Band Part Block Diagram



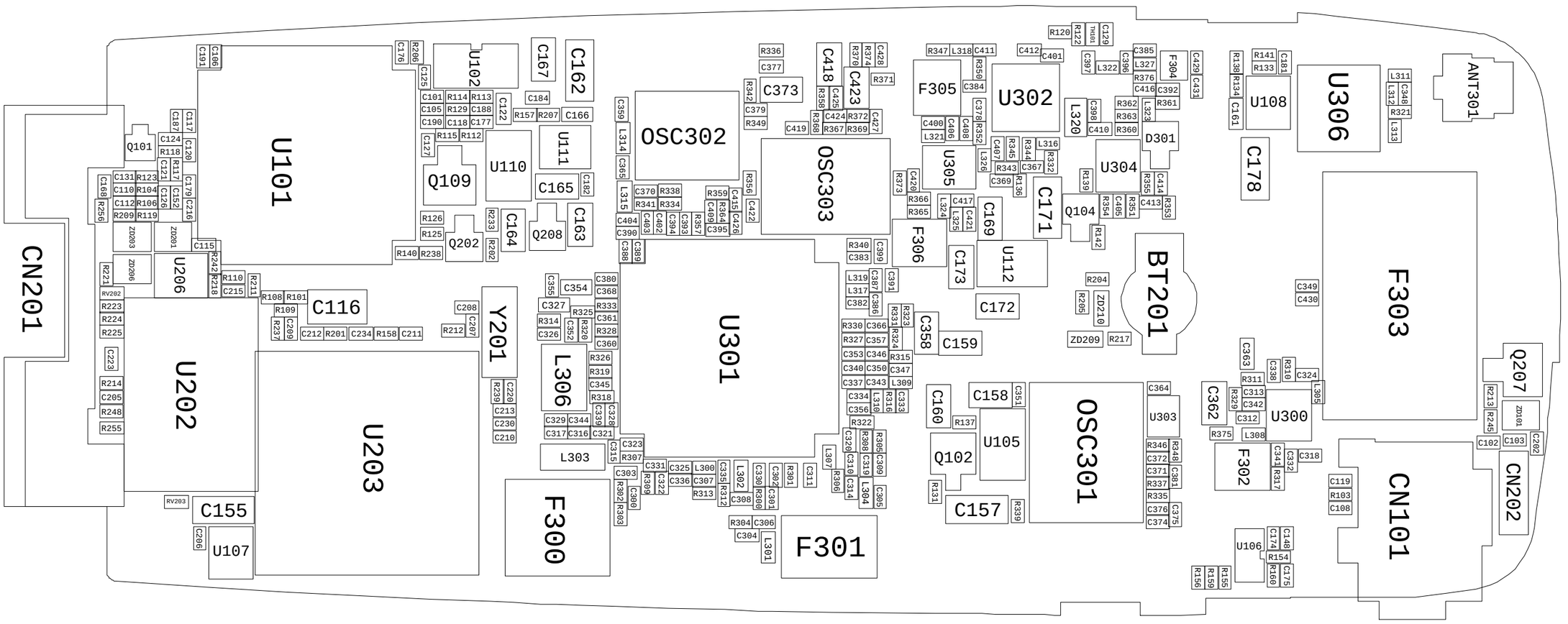
2. Radio Part Block Diagram



1. Main PCB Top Diagram



2. Main PCB Bottom Diagram



6. STH-N375 Circuit Description & Circuit Diagrams

STH-N375/N371 provides the AMPS and the Digital TDMA (cellular band only) of compliance with TIA/EIA/IS-136. The radio operation of the STH-N375N371 has been implemented with the receiver, the transmitter, and the local oscillator controlled by the PLL. The circuit of the STH-N375/N371 is described as followings.

1. Baseband Section

1-1. Power Supply

For the POWER ON, with the battery installed on the telephone and by pressing the END key, the BATT and ON_SW signals will be connected, which it will turn on Q107. In addition, Q106 is turned on by Q107, and thus the BATT is connected to VBAT. Consequently, VBAT is supplied to input of regulators U107, U110 and U111. The regulator U110 supplies all powers of baseband part (VCC, AVCC, V_VCTCXO). The regulator U111 supplies IVCC (2.2 V) to Baseband Engine Chip (U203: BEC). The regulator U107 supplies VAUX (3.3V output power) to LED for back-light of U312. After the BEC (U203) is supplied power from VCC, IVCC. The BEC use 14.4MHz as reference clock, 14.4MHz comes out from TCXO (OSC302). If the powers (VCC,AVCC, V_VCTCXO) and reference clock are normal, the main application program will start to run. In addition, the BEC starts to run and outputs OWER_HOLD signal (low active), which is connected to Q105. Moreover, Q105, Q106 and Q107 are turned on in order. In consequence, BATT is connected to VBAT continuously although END key is released (ON_SW disconnected BATT). The powers from U110 and U111 are used in all baseband part of BEC, IFC (Interface Chip U101).

For the POWER OFF, in this case main application program is running already. The main application program check all GPIO inputs periodically. The END key is pressed during program run, the BATT and ON_SW signals will be connected. This turns on Q108. Therefore, ON_SW_SENSE that is connected to GPIO_0_5 (U203_ C13) turned logic high to low. The BEC checks this signal, main application program enter to POWER OFF mode.

1-2. BEC (U203) interface

BEC (U203) mainly consist of two parts HOST CPU and Baseband Engine (Figure2~1). This is the most important component of dual-mode (US-TDMA and AMPS mode) cellular telephone. It has IKx32bits of internal ROM and 2Kx32bits of internal RAM. This chip communicates with a lot of peripheral device, memory (SRAM, ROM), Key-Matrix and display module. The BEC receives TCXO clock signals (reference clock) from the TCXO and controls the telephone during the operation. The BEC communicates with the IFC through several serial links. These include CODEC, wideband data, receiver data, transmitter data, and auxiliary data interface. A master baseband clock (BBCLK: U203_H2) at either 6.2208 MHz or 5.12 MHz or 4.096 MHz, depending on the operating mode, from the BEC drives the IFC. The major components are as follows:

Separate address and data buses provide a data path to external memory and memory-mapped peripherals. The 22-bit address bus provides a byte addressing range up to 8 MB in each of 4 spaces decoded by the 4 select signals. The 16-bit data bus in conjunction with the UBE signal allows word or byte transfers. Table2-1 shows the ARM memory map. An Intel 28F3204 Stacked Memory chip supplies 4M Bytes of Flash memory and 512K Bytes of SRAM. Note that in the telephone, the SRAM is located at the CS_RES1 block of memory.

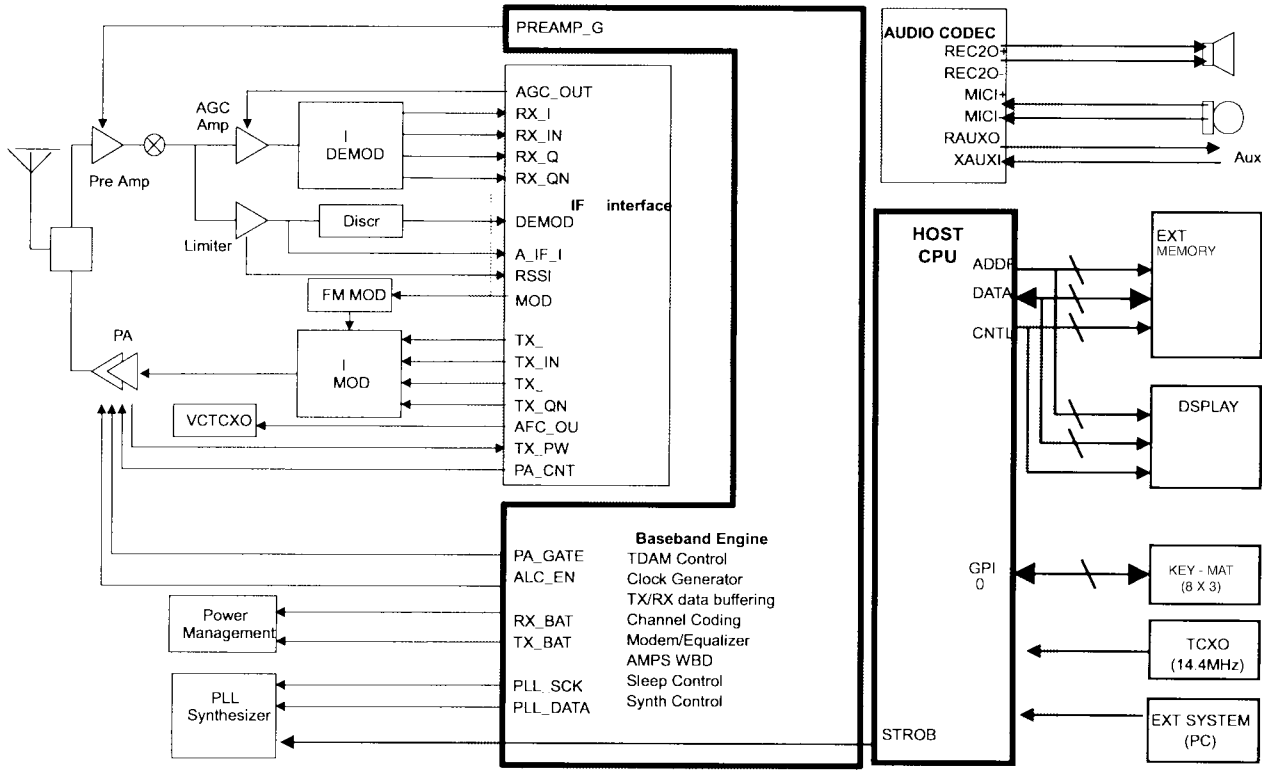


Figure1. BEC interface and block diagram

Table1. ARM Memory Map

ARM Memory Map						
ARM Address Range		Data	Block Size Bytes	D5206_LIB Name	APP_PIN Name	Remarks
0000 0000	0000 0003	32	4 Byte	Internal ROM	-	R
0000 0004	0000 1FFF	32	8K Byte	Internal RAM	-	R/W
0002 0000	0002 0FFF	32	4K Byte	Internal ROM	-	R
0004 0000	0005 FFFF	32/16	NA	Internal Peripherals	-	R/W
0080 0000	00FF FFFF	8/16	Up to 8 M Byte	FLASH_CS	FLASH_CS	R/W
0100 0000	017F FFFF	8/16	Up to 8 M Byte	SRAM_CS		R/W
0180 0000	01FF FFFF	8/16	Up to 8 M Byte	CS_RES1	SRAM_CS	R/W
0200 0000	027F FFFF	8/16	Up to 8 M Byte	CS_RES2	DISPLAY_CS	R/W

HOST CPU (inside of BEC:U203)

ARM7TDM1 32-bit microprocessor is used for the main call processing. The CPU controls all the circuitry. The reference clock 14.4 MHz, coming from the output of the TCXO (OSC302), is connected to VCTCXO_IN (pin F3). For the sleep mode, additional crystal oscillator (Y201) of 32.768kHz is connected to pin B2 of the BEC. The interface circuitry consists of reset circuit, address bus (A0-A21), data bus (AD0-AD15), control signals (MEMWEB, MEMOEB, SRAM_CS, FLASH CS, DISPLAY_CS, UBE etc), GPIOs, and the communication ports. The communication ports includes UARTI, UART2, JTAG, and SCI. The UARTI supports HP equipment interface, down loading, and data service. The UART2 and the JTAG are used for the software debugging. The SCI ports support the diagnostic monitor (DM) function.

FLASH ROM (inside of U202)

The 16Mbits FLASH ROM is used to store code of the application program. Using the down-loader program, this application program can be changed even after the mobile is fully assembled.

SRAM (inside of U202)

The 4Mbits SRAM is used to store the internal flag information, call processing data, and timer data.

Key-Matrix

The Key-Matrix is consisted of 8 x 3 matrix, which use GPIO input signal SCAN0-7 and GPIO output signal KEY0-2 of BEC.

LCD MODULE

LCD module is connected to main board directly. This contains 4-LEDs they are used as backlight. The LCD controllers control the information of displaying from the BEC (parallel 8-bit data) to the LCD.

BASEBAND ENGIN (inside of U203)

This part mainly interfaces with IFC (U101) and RF part. As for interface of IFC, that will be explained detail in next section. As important signals are PREAMP_G for receiver path, PAGATE, ALC_EN for transmitter path, PLL DATA, PLL CLK, PLL STRBl for PLL synthesizer, RX BAT, TX BAT for power management.

1-3. IF INTERFACE CHIP (IFC: U101)

The IFC provides the radio IF and audio interfaces (Figure2-2). Differential Rx l/Q and Tx l/Q signal pairs interface directly with the RF interface chip (RFIC: U301) device. MOD, AFC, AGC, RSSI, and PA CNT signals also directly control the radio circuitry. Three audio paths are implemented. The primary path utilizes the microphone and speaker, located on the main board. Both microphone and speaker utilize the main differential circuits in the IFC to minimize noise pickup. The speaker output is amplified internally to enable direct connection to the speaker. The second audio path connects to the headset jack. The headset microphone and speaker are passed to the IFC's auxiliary input and output, respectively. The headset jack terminals indicate via the HEADSET SENSE line when the headset is present as well as when the headset button is pushed via the SEND END line. The third audio path to the HFK shares the auxiliary output with the headset for its speaker and uses the second auxiliary input for its microphone. Since the auxiliary output is not internally amplified, an external audio amplifier is applied before connection to the headset and HFK.

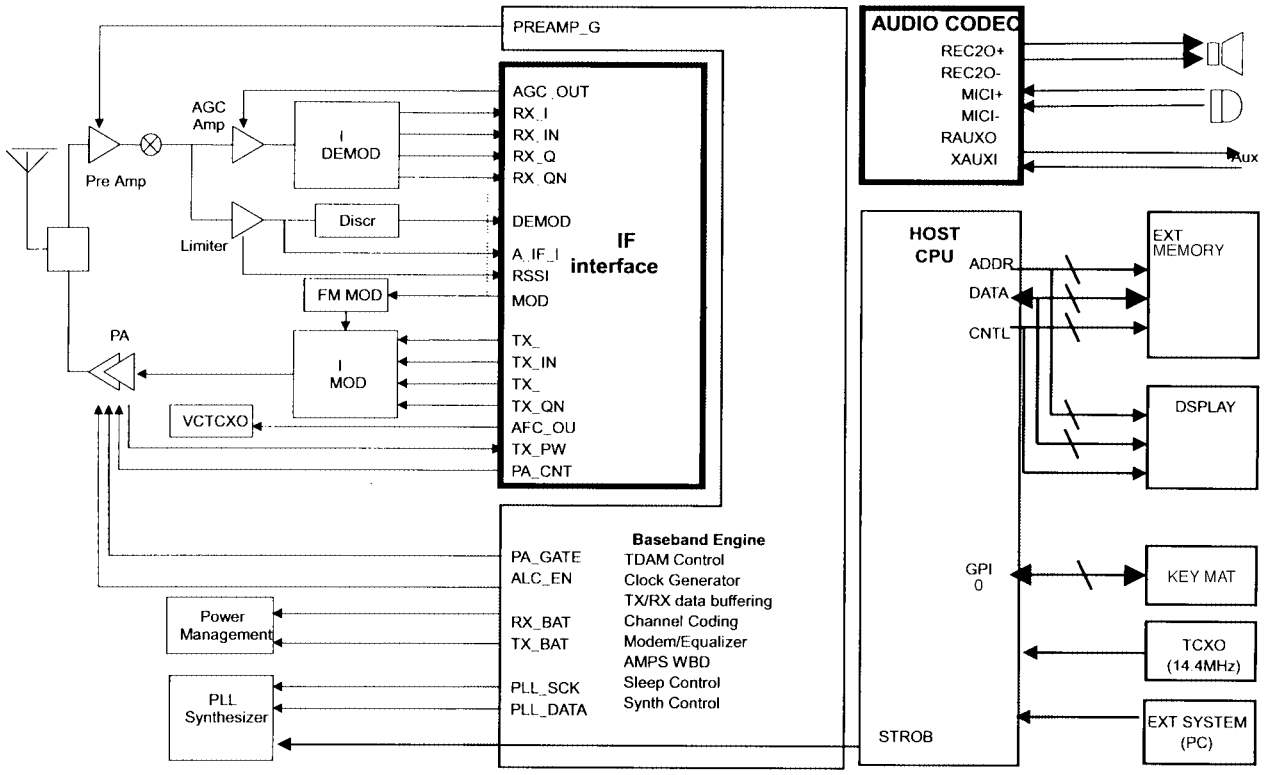


Figure 2. IFC interface and block diagram

The IFC (Ul 01) is mainly consist of IF interface part and AUDIO CODEC part. The IF interface part, witch is between RF part (mainly U301) and BEC, translate RF data to baseband data for BEC. Mainly, IF interface part is consist of receiver, transmitter, and some kind of RF control. The IFC also provides several A/D inputs to monitor system parameters. Battery voltage is periodically measured after scaling via a resistor divider (BAT MON: U101_67). A thermistor located near the PA is monitored to obtain temperature status by TMP MON (U101 66).

Receiver interface

The U101 receive differential 1/Q signals (RX_IN, RX_I, RX_QN, RX Q: U101 48,49,5O,51), or DEMOD signal (U101_52) which come from RF demodulator (U301_11,12,9,10,16), and translate as digital data. These data is synchronized by control signals (RX_SYNC, RX CLK, and BBCLK: U101 31,32,40) is transported to BEC through RX DATA (pin U101_30). in addition, the U101 uses AGC_OUT (U101 72) for dynamic range of receiver signal strength connected to U301_17, AFC_OUT (U101_71) for adjusting reference frequency exactly connected to TXCO (OSC302 1).

Transmitter interface

The U101 receives TX DATAI (U101 36) synchronized by control signals (TX SYNC, TX_CLK: U101_33,34), which come from BEC, and translate this data as differential l/Q signals (TX_IN, TX 1, TX_QN, TX Q: U101_61,60,58,57), or MOD signal (U101_63). it transports these data to RF modulation part. In addition, the U101 uses PA CNT (U101_73),TX PWR (U101 68) for controlling power of transmitter.

AUDIO CODEC

Three audio paths are implemented in IFC. The primary path utilizes the microphone (U101_11,12) and speaker (U 101_77,79). Both microphone and speaker utilize the main differentiai circuits in the IFC to minimize noise pickup. The speaker output is amplified internally to enable direct connection to the speaker. The second audio path connects to the headset jack. The headset microphone and speaker are passed to the IFC's auxiliary input (U101_5) and output (U101_2), respectively. The headset jack terminals indicate via the HS_SENSE (U106-2_7) to GPIO of BEC (U203_C11) when the headset is present. As well as when the headset button is pushed via the SEND END (U106-1_1) to GPIO of BEC (U203 A13). The third audio path to the HFK shares the auxiliary output with the headset for its speaker and uses the second auxiliary input for its microphone. Since the auxiliary output is not internally amplified, an external audio amplifier (U102) is applied before connection to the headset and HFK.

2. RF Section

2-1.Introduction

For playing essential role in the radio part, STH-N375 N371 includes many active components. They are U300 (LNA), U302 (Cellular band power amplifier), U301 (transceiver including up / down converter, RF and IF PLLs, Rx and Tx AGCs, IQ modulator and demodulator, limiter, and discriminator), OSC301 (RF VCO), and OSC303 (TXIF VCO). in order to obtain good RX selectivity and sensitivity simultaneously, STH-N375 N371 has dual IF conversion system. The 1st IF and 2nd IF are 130.05 MHz and 450 kHz, respectively.

2-2.Front-End part

RF signal from the air interface passes U306 (RF test switch) and F303 (duplexer). The purpose of U306 is to couple the RF signal and test on the conduction line. F303 plays the role of Rx and Tx filtering and the isolation between Rx and Tx in the cellular band (AMPS and Digital TDMA).

2-3.Reeeiver

The Rx signal from F306 goes into U300. U300 amplifies the very weak Rx signal with adding the negligible thermal noise. U300 features 20dB gain, 1.3 dB NF, and 7mA current consumption. For the wider dynamic Rx AGC (automatic gain controller) range, the gain of U300 is controlled by PREAMP_G signal coming from U203, resulting in around 30-dB step gain change. By checking the RSSI through U101_69, U203 decides to whether turn on U300 or not. The amplified signal goes into F302 (RF SAW filter) in order to suppress the unwanted band data.

The signal coming out from F302 inflows to the pin 45 (Ist Rx mixer input) of U301, and it is downconverted to the IF of 130.05 MHz. This 1st mixer has around 7dB conversion gain, 6dB NF, and 5dBm IIP3. For the downconversion, the local frequency source from OSC301 (dual RF VCO) is used. For the local frequency, the Rx frequency plus 1st IF (that is, high injection type local frequency) is used, and this frequency is controlled by the RF PLL in U301 in conjunction with U203 (baseband IC)

The 1st mixer output is connected to F301 (130.05 MHz 1st IF SAW filter). The main role of F301 is suppression of undesirable interferers. For the 2nd IF conversion, the output of F301 is connected to the 2nd Rx mixer of U301. The 2nd mixer has the typical characteristics of 13.5 dB gain, 12 dB NF, and -20dBm IIP3. The local frequency source for making 2nd downconversion is supplied from U301 internally by 9 times multiplying the fundamental frequency of OSC302 (14.4MHz VC-TCXO). The downconverted signal passes F300 (450 kHz Ceramic filter) in order to suppress the unwanted interferers and the image frequency signals.

Until now, the Rx signal path is common for both of AMPS and Digital TDMA. From the filtered 450 kHz signal output, AMPS path and TDMA path come to separate for proper treating of the Rx signal. To begin with, AMPS path will be described.

AMPS (Limiting and Discrimination)

The downconverted signal from the output of F300 enters to the limiter and discriminator of U301. For the better suppression of the unwanted interferers, discrete LC filter is used in the limiter section. The signal through the limiter goes into the discriminator (or quadrature detector) of U301 with incorporation of the quadrature tank circuit (LC resonator) placed outside of U301, and thus the audio signal comes out from the pin 16 of U301. This demodulated signal is connected to U101.

TDMA (Rx AGC and 1, Q Demodulator)

The downconverted signal from the output of F300 enters to the Rx AGC and 1, Q demodulator of U301. The Rx AGC has the performance of 80-dB dynamic range, 10 dB NF, and -85dBm IIP3. In the process of 1, Q demodulation, 450 kHz local signal, made by dividing 14.4 MHz reference clock, is used.

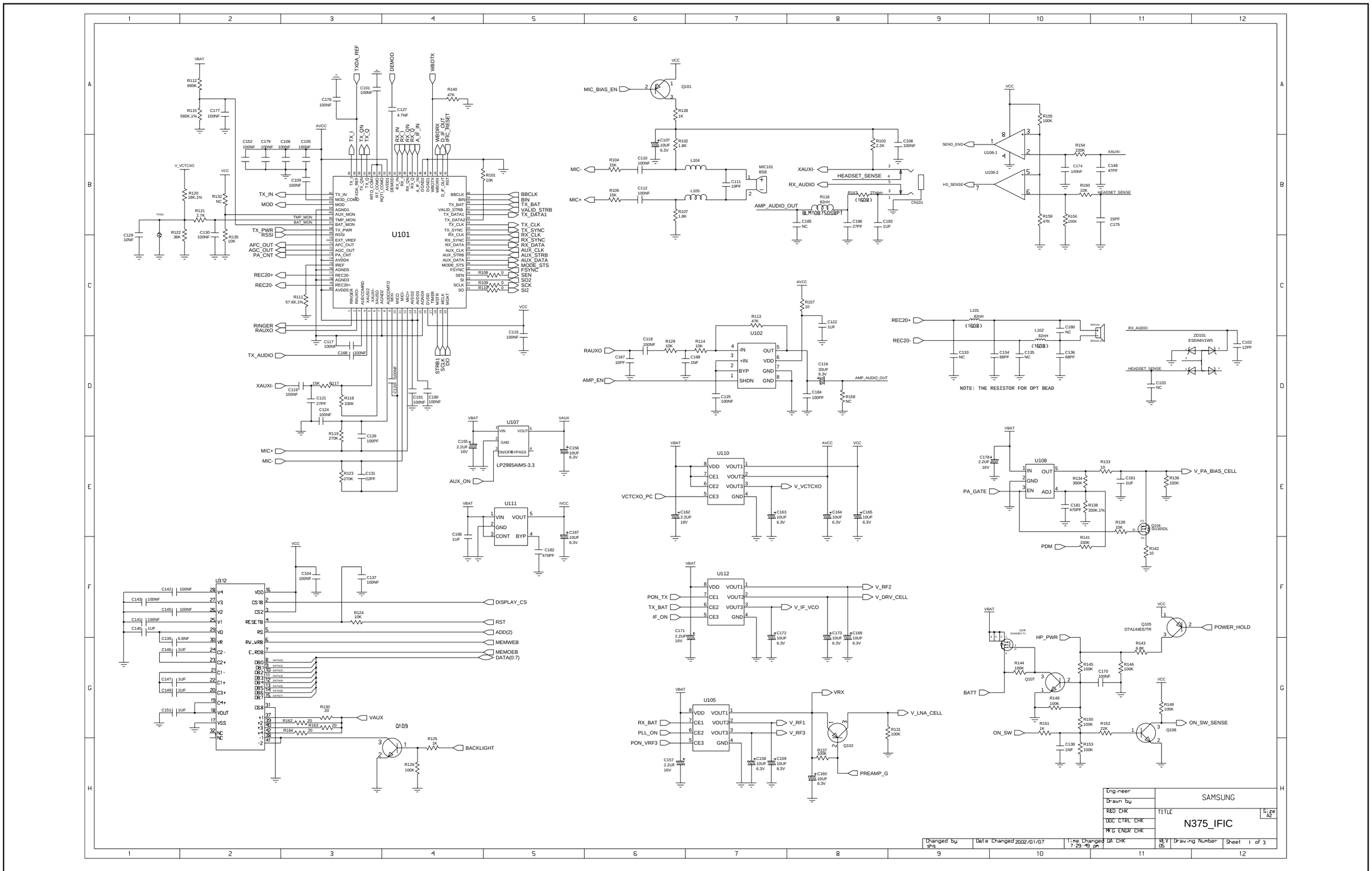
2-5. Radio component control

U101 monitors the state of the radio part, and delivers the information to U203. Then, U203 sends the proper control signals to radio relating regulators and AGCs. The radio interface signals are summarized in the Table 2-2.

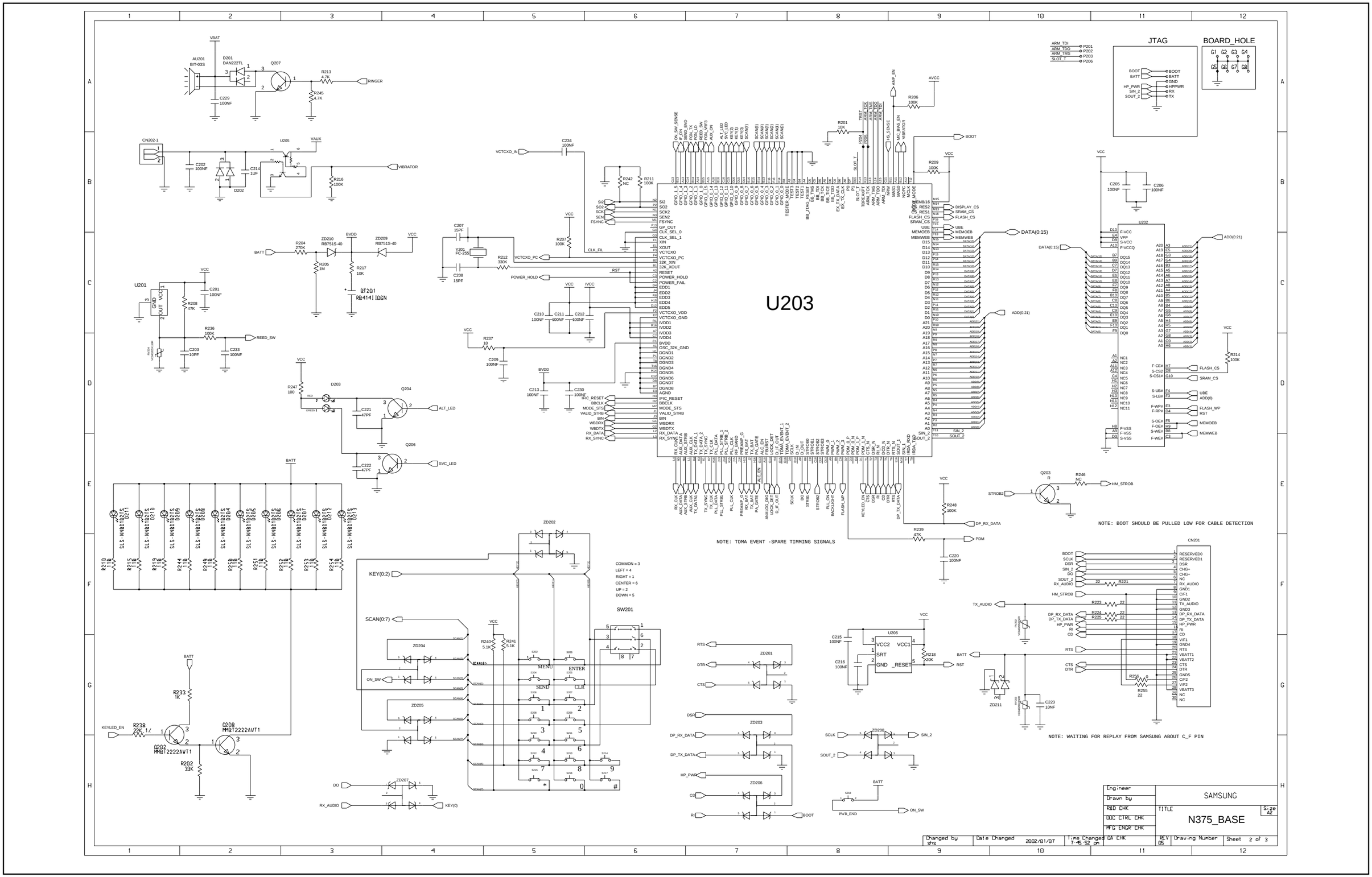
Table 2-2. Radio Interface Signals

Signal Name	Source/Destination	Function
PON_LD	BEC / RFIC	Limiter / Discriminator power control
TX_RFBAND	BEC / IF VCO	Tx band control (0=PCS, 1=Cell)
VCTCXO_IN	TCXO / BEC	14.4 MHz clock
VCTCXO_PC	BEC / TCXO	14.4 MHz clock power control
PLL_DATA	BEC / RFIC	PLL serial data
PLL_CLK	BEC / RFIC	PLL serial clock
PLL_STRB1	BEC / RFIC	PLL serial strobe
RF_BAND	BEC / Various	Cell / PCS band select (0=Cell, 1=PCS)
PREAMP_G	BEC / Regulator	Rx AGC Gain step
RX_BAT	BEC / RFIC & Various	Receiver power control
TX_BAT	BEC / RFIC & Various	Transmitter power control
ANALOG_DIG	BEC / Various	Band control (0=Analog, 1=Digital)
LOCK_DET	RFIC / BEC	PLL lock detect status
PLL_ON	BEC / Regulator	PLL power control(V_RF1:RFIC)
A_IF_IN	RFIC / IFC	IF comparator input
RX_Q, RX_QN	RFIC / IFC	Differential analog receive Q channel
RX_I, RX_IN	RFIC / IFC	Differential analog receive I channel
TX_Q, TX_QN	IFC / RFIC	Differential analog transmit Q channel
TX_I, TX_IN	IFC / RFIC	Differential analog transmit I channel
MOD	IFC / RFIC	Drive to modulator
TX_PWR	Detector / IFC	Tx power detector
RSSI	RFIC / IFC	Rx Signal Strength Indicator
AFC_OUT	IFC / VCTCXO	Auto Frequency Control voltage
AGC_OUT	IFC / RFIC	Auto Gain Control voltage
PA_CNT	IFC / RFIC	Power Amplifier control voltage
DEMOD	RFIC / IFC	Discriminator output
TXDA_REF	RFIC / IFC	Tx section common mode DC bias
PON_TX	BEC / Regulator	TX up converter power (V_RF2:RFIC)
PON_VRF3	BEC / Regulator	Local Amp power(V_RF3:RFIC)

3. IFIC Circuit Diagram

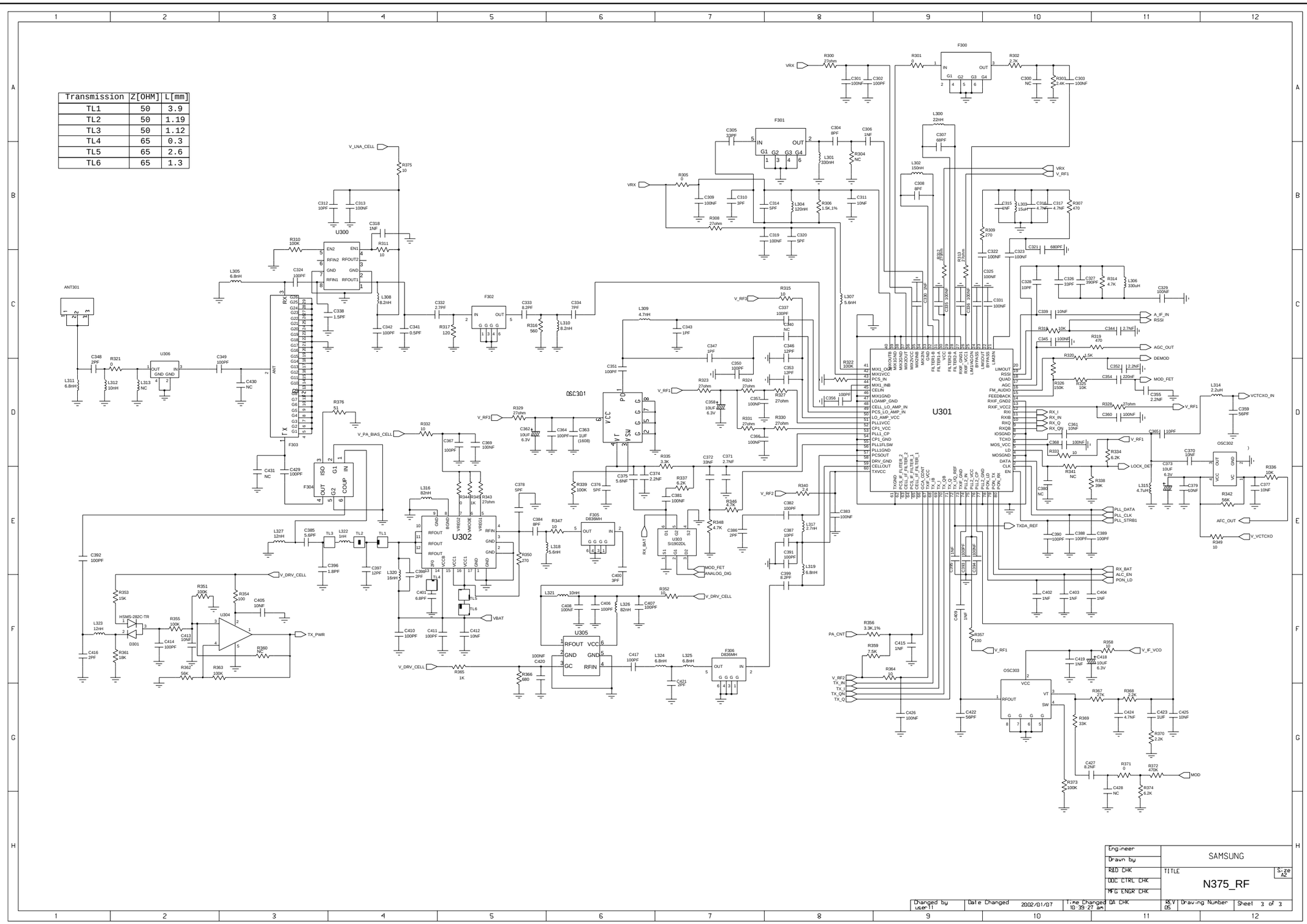


4. BASE Circuit Diagram



5. RF Circuit Diagram

Transmission	Z[OHM]	L[mm]
TL1	50	3.9
TL2	50	1.19
TL3	50	1.12
TL4	65	0.3
TL5	65	2.6
TL6	65	1.3



Engineer		SAMSUNG	
Drawn by			
R&D CHK		TITLE	Size A2
DOC CTRL CHK		N375_RF	
MFG ENGR CHK			
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REV 05	Drawing Number	Sheet 3 of 3	