3. SGH-P207 Circuit Description

1) RF Circuit Description of SGH-P207

1. FEM (F401)

==> Switching Tx, Rx path for GSM850, DCS1800 and PCS1900 controlled by logic.
Integration of GSM850, DCS1800 and PCS1900 RX SAW Filters.
To convert Electromagnetic Field Wave to Acoustic Wave and the pass the specific frequency band.
- for filtering the frequency band 824 ~ 849 / 869~ 894 MHz
- for filtering the frequency band 1710 ~ 1785 / 1805 ~ 1880 MHz
- for filtering the frequency band 1850 ~ 1910 / 1930 ~ 1990 MHz

2. FEM Control Logic

==> Truth Table

	VC1	VC2	VC3
GSM850 Tx Mode	**H**	**L**	**L**
DCS/PCS Tx Mode	**L**	**H**	**H**
PCS Rx Mode	**L**	**L**	**H**
GSM850/DCS Rx Mode	**L**	**L**	**L**

3. VC-TCXO(OSC401)

==> To generate the 26 MHz reference clock to drive the logic and RF.
After additional process, the reference clock applies to the U603 VCXOB pin to modulate TXIQ and demodulate RXIQ.

4. HD155154NP (U401)

==> The HD155154NP is a RF tranceiver IC for GS850, DCS1800 and PCS1900 triple band cellular systems, and incorporates EDGE tranceiver capabillity, and integrates most of the low power silicon functions of a tranceiver.
The HD155154NP incorporates triple RF LNAs, direct conversion mixers which are IQ demodulator, an auto offset calibrated programmable gain amplifier with baseband filter for both IQ chains, RF architecture for the transmitter.
Moreover the HD155154NP includes power mode controller to optimize the power consumption. These functions can operate down to 2.7V and are housed in a 48-pin DPE QFN SMD package.

- RX Function
  - Differential Low Noise Amplifiers
  - Direct Conversion mixer and IQ demodulator with 90 degree phase splitter.

- Auto offset calibrated programmable gain amplifier with baseband filter(PGA)

- TX Function
  - I/Q modulator with 90degree phase splitter
  - Offset PLL
    - Phase comparator included fast lock system (Digital phase detector)

  - Polar loop
    - Lineariser
    - Voltage gain amplifier
    - Inverse voltage gain amplifier
    - Down converter
    - AM detector
  - PLL Synthesiser
    - RF Synthesiser for RX/TX RF local included fast lock system
    - 400kHz comparison frequency to achieve faster lock-up time

5. POWER AMP (U404)

==> The PF09016B is a high-power, high-efficiency power amplifier module with integrated power control

- Quad band Polar Loop Amplifier for GSM850 (824 to 849 MHz), GSM900(880 to 915 MHz), DCS1800(1710 to 1785 MHz) and PCS1900 (1850 to 1910 MHz).
- For 3.5 V normal operation
- Built in LDO
- Superb output linearity
- High gain 3-stage amplifier : +5dBm input typical
- GPRS / EGPRS Operation Compatible
- Small package : 8.0 X 13.75 mm

2) Baseband Circuit Description of SGH-P207

1. CSP2750 (U101)

==> The CSP2750 has two major logical components power management and conversion
signal processing.

The PSC component is responsible for all power-related functionality, including the following;

- Power management for RF, BB and ancillary devices within the GSM/GPRS
- Battery-charge management
- Reset control
- SIM card voltage-level shifting

The CSP component is responsible for the following ;

- Intraframe event scheduling
- Voice band processing, including voice band ADC and DAC
- Analog baseband processing, including baseband ADC and DAC
- Providing RF interface for Trident digital baseband device
- Transmitter Power control
- Automatic frequency control
- A5 ciphering
- Low-power sleep mode and wake-up control

The CSP2750 has the following major physical components;

- Timing and control unit
- RF serial interface
- Low-power sleep mode controller
- Baseband Transmitter / Receiver
- Voice input and output

2.UPD9993(U102)

==> The UPD9993 is a mobile phone ring tone generator and MP3/AAC decoder LSI that includes an on-chip realtime surround function.

- PCM sound generation method provides realistic sound reproduction.
- Built in Digital Signal Processor for MP3/AAC decoder.
- Built in Real Time Surround Processor.
- Built in Real Time Surround Processor.

(for all sources including PCM sound generators, MP3/AAC source, and audio serial input).

- Up to 68 tones can be played at the same time, so an abundant variety of tunes can be generated and played.
- Supports ADPCM playback. Simultaneous playback with MIDI is also available.
- Includes a High-performance D/A converter with 16-bit resolution
- Supports five sampling frequency modes: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz (ASI only)
- Provides audio serial I/O interface (16 bits). The serial data input frequency is variable between 32 fs and 64 fs(during slave mode). Supported formats are right-justified, left-justified, and IIS.
- Includes function for mixing MIDI/ADPCM/MP3/AAC signals and audio serial input signals (only fs = 32 kHz sampling is supported).
- Supports 8 bit Parallel Interface**.** Host CPU is connected via an 8-bit parallel interface when PS=0.
- Supports SPI**.** Host CPU is connected via a 3 wire or a 4 wire Serial Peripheral Interface (SPI) when PS=1.
- Supports MONO output. It is possible to output differential mono signals.
- Includes output control functions for vibration and LED
- Built in PLL, so various types of input clocks can be supported.
- Supports two I/O power supply voltages: 3 V and 1.8 V

(supports only digital pins)

- Power supply voltages:

  DVDD : 1.425 to 1.575 V

  EVDD : 1.71 to 3.3 V

  AVDD : 2.7 to 3.3 V

  AVDD_P : 2.7 to 3.3 V
- 85-pin tape FBGA package (6 × 6 mm body size, 0.5 ball pitch)

3. TRIDENT-HPE(U201)

==> The Trident-HPE digital baseband processor is a complete system IC designed for wireless terminals that includes two digital signal processor(DSP) cores optimized for low-power communications applications and a powerful, high-performance, industry-standard microcontroller core along with a rich set of peripherals.

The Trident-HPE digital baseband processor achieves best-in-class signal processing performance while maintaining the efficient software code density, low power consumption, and small physical size required for GSM/GPRS terminals

ARM946E-S microcontroller core;

- 101 MHz system bus, 16 kbyte instruction and 16kbyte data caches.
- 8 kbyte tightly coupled zero wait-state instruction and 4kbyte tightly coupled zero wait-state data memory
- direct memory access controller for transparent transfer between memory and peripherals.
- External Memory interface with asynchronous burst mode support
- Synchronous serial port supporting
- Programmable 48-bit general-purpose IO unit, keyboard interface, programmable interval timer and real-time clock.
- SD/MMC controller that supports interfacing to secure digital/multimedia memory card.

Two DSP16000 dual-MAC DSP cores;

- Up to 404 million MACs per second at 101 MHz.
- Memory complement;
  - DSP0 : 144K X 16-bit ROM, 40k X 16-bit RAM.
  - DSP1 : 96K X 16-bit ROM, 16k X 16-bit RAM.

JTAG boundary scan and integrated H/W developement system

Low power;

- Ultralow leakage process technology for best-in-class standby power
- Flexible power management modes to allow for maximum active power management

Interprocessor communication hardware support between ARM, DSP0 and DSP1.

Supported by Trident-HPE digital baseband processor software and hardware developement tools as well as industry standard ARM software and hardware developement tools

Two on-chip, programmable, PLL clock synthesizers;

- one for ARM and DSP, the other one for USB.

4. CL701A4(U301)

==> The CL701A4 is the high-technology from CORE LOGIC that expands scope to Mega Pixel solutions.

It is a low power-consuming single chip controller, optimized to provide highly advanced digital camera functions, including camcorder features through a small LCD of mobile devices, with the minimal technical difficulty. The CL701A4 supports Standard SRAM Interface for the interface with modem CPU, which allows easy control of the chip through Read/Write registers.

The CL701A4 is stacked with 4Mbit, expandable to 32Mbit, SRAM, equipped with built-in JPEG and Motion-JPEG H/W CODEC.

In addition, the CL701A4 supports various types of STN/TFT/OLED LCD Driver Controllers of 8-bpp*, 12-bpp, 16-bpp,and 18-bpp color depths. With the built-in CMOSbased/CCD Image Sensor Controller, which supports CCIR601 and CCIR656 formats, the CL701A4 enables mobile devices to accomplish variety of digital camera functions.

Key camera and camcorder functions of the CL701A4 include linear (Over 90 steps) real digital 4x zoom for previews of moving images, OSD images, and Captured Still Images via-OSD, Single-Shot Still Images, Motion-JPEG Images (Mini Movie Preview), and images captured through Continuous Shooting.

To accomplish minimum power consumption, the CL701A4 provides Bypass Mode that can be controlled by using M_HOLD signal. In such a case, Modem CPU directly controls LCD. Otherwise, Modem CPU lets the CL701A4 to control LCD for camera functions under camera mode. For proper operation of the CL701A4, it requires maximum input frequency of 27MHz. And for determining image frame rate, it vastly depends on input clock frequency and proper settings of related registers.