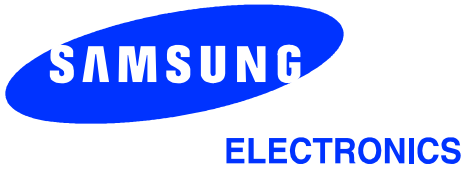
SAMSUNG

SAMSUNG Anycall
SGH-N700

SERVICE Manual

SAMSUNG Anycall

CONTENTS



ELECTRONICS

Code No.: GH68-06532A
BASIC.

1. SGH-N700 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880
ARFCN range	1~124	0~124 & 975~1023	512~885
Tx/Rx spacing	45MHz	45MHz	95MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	35Km	2Km

2. GSM TX power class

TX Power control level	GSM900
5	33±2 dBm
6	31±2 dBm
7	29±2 dBm
8	27±2 dBm
9	25±2 dBm
10	23±2 dBm
11	21±2 dBm
12	19±2 dBm
13	17±2 dBm
14	15±2 dBm
15	13±2 dBm
16	11±3 dBm
17	9±3dBm
18	7±3 dBm
19	5±3 dBm

TX Power control level	DCS1800
0	30±2 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

2. SGH-N700 Circuit Description

1. SGH-N700 RF Circuit Description

1) RX PART

1. FEM(U402(SWITCHPLEXER+FILTER)) → Switching Tx, Rx path for E`GSM900, and DCS1800 by logic controlling.

2. FEM Control Logic (U402) → Truth Table

	VC1	VC2
DCS / PCS Tx Mode	L	H
GSM Tx Mode	H	L
GSM / DCS Rx Mode	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (U402(SWITCHPLEXER+FILTER)) → For filtering the frequency band between 925 ~ 960 MHz
- DCS FILTER(U402(SWITCHPLEXER+FILTER)) → For filtering the frequency band 1805 and 1880 MHz.

4. VC-TCXO (OSC401)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U900 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. SI 4205 (U404)

This chip integrates two differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from frequency synthesizer. The RFLO frequency is between 1849.8~1879.9MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

Also, this chip down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U404 chip.
SI4205 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U403).
The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc

2. Baseband Circuit description of SGH-N700

1) CSP2200B1

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity. A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the CSP2200B1 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register. Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps.

Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

4. Vibrator Motor Driver

The vibrator motor driver is a independent voltage regulator to drive a small dc motor that silently alerts the user of an incoming call. The driver is a 3.0V constant source while sinking up to 180mA and controlled by enable signal of main chip. For efficient use and safety, the vibrator motor should be connected between the regulator output and the ground.

2). LCD

LCD is consisted of main LCD(B/W STN LCD). Chip select signals of EMI part in the trident, LCD_CS, can enable main LCD. VDD_EL signal enables EL of main LCD. In sleep mode, EL are turned off.
These two signals are from IO part of the DSP in the trident. RST signal from CSP2200B1 initiates the initial process of the LCD.
8-bit data lines(D(0)~D(7)) transfers data and commands to LCD . Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data.
The signals which inform the input or output state to LCD, are required. But this system is not necessary for read enable signal. CP_WEN signal is only used to write data or commands to LCD.
Power signal for operating LCD driver is VCCD.

3). JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.
CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

4). Keypad

This is consisted of key interface pins in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix.
So power on/off signal is connected with CSP2200 to enable CSP2200.

5) IF connetor

It is 18-pin connector, and separated into two parts. One is a power supply part for main system. And the other is designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, TA, VF, and GND. They connected to power supply IC, microprocessor and signal processor IC.

6) Audio

AOUTAP, AOUTAN from CSP2200 is connected to the speaker via analog switch. MICIN and MICOUT are connected to the main MIC.
YMU759 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU759 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU759 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.
YMU759 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.

7) Memory

This system uses AMD's memory, **S71JL064HA0BAW110**.
It is consisted of 64M bits flash memory and 16M bits PSRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP2200. It has 22 bit address lines, A[0~21]. They are also connected. CP_CSROMEN signal, chip select signal in the trident, enable flash memories. They use 2.8 volt supply voltage, VCCD.
During wrting process, CP_WEN is low and it enables writing process to flash memory and PSRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or PSRAM to data lines. Each chip select signals in the trident select flash memory or PSRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use RST. A[0] signal enables lower byte of PSRAM and UPPER_BYTE signal enables higher byte of PSRAM.

8) Trident

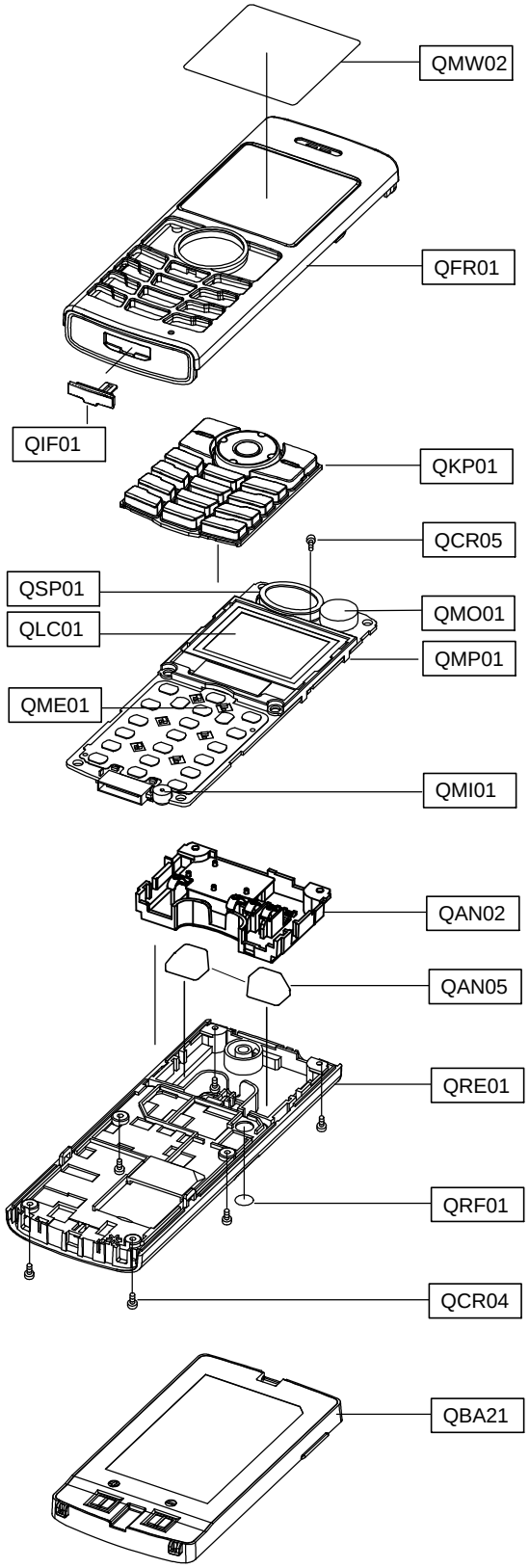
Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.
DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP2200. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762.
ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.
CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.
Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communications using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).
And UP_CS/SCLK/SDI, control signals for CSP2200 are outputted through PPI pins. It has signal port for charging(CHG_DET), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

8) X-TAL(13MHz)

This system uses the 13MHz TCXO. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. This clock is fed to CSP1093,Trident,YMU759 and Silab solution.

3. SGH-N700 Exploded Views and Parts List

1. Cellular phone Exploded View-1



2. Cellular phone Parts list

Location NO.		Description	SEC CODE	Remark
QMW02		PMO-MAIN WINDOW	GH72-13316A	
QFR01		MEC-FRONT COVER	GH75-04537A	
QIF01		PMO-IF COVER	GH72-16745A	
QKP01		MEC-KEYPAD ASSY	GH75-04539A	
QSP01		SPEAKER	3001-001576	
QMO01		MOTOR	GH31-00047A	
QMP01		MIAN PBA	GH92-01986A	
QLC01		LCD	GH07-00623A	
QME01		UNIT METAL DOME	GH59-01456A	
QMI01		MICROPHONE ASSY	GH30-00125A	
QCR05		SCREW	6001-001478	
QAN05		MEC-INTENA RUBBER	GH75-05620A	
QRE01		REAR COVER	GH75-04538A	
QCR04		SCREW-MACHINE	6001-001479	
QRF01		MPR-R/F COVER	GH74-08243A	
QBA21		BATTERY-820MAH	GH43-01599A	
QAN02		INTENNA	GH42-00444A	

3. Test Jig (GH80-00865A)

3-1. RF Test Cable
(GH39-00182A)

3-2. Test Cable
(GH39-00127A)

3-3. Serial Cable

3-4. Power Supply Cable

3-5. DATA CABLE
(GH39-00143B)

3-6. TA
(GH44-00284A)

4. SGH-N700 Electrical Parts List

SEC CODE	Design LOC
0403-001387	ZD629
0403-001427	ZD628
0403-001511	ZD301
0404-001172	D501
0406-001150	ZD501
0406-001150	ZD502
0501-000481	Q301
0504-001113	Q102
0601-001094	LED601
0601-001094	LED602
0601-001094	LED605
0601-001094	LED606
0601-001094	LED607
0601-001094	LED608
0601-001094	LED631
0601-001094	LED632
0601-001094	LED633
0601-001094	LED634
0601-001094	LED635
0601-001094	LED636
0601-001956	LED610
0801-000796	U102
1001-001261	U501
1003-001395	U302
1109-001309	U202
1201-002177	U403
1203-001917	U601
1203-003109	U107
1203-003304	U101
1204-001811	U502
1205-002433	U404
1209-001219	U203
1405-001082	ZD601
1405-001082	ZD602
1405-001082	ZD603
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1405-001082	ZD606
1405-001082	ZD607

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1405-001082	ZD619
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2007-000138	R424
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2007-000164	R504
2007-000171	R102
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2007-001292	R503
2007-001319	R101
2007-001325	R507
2007-002797	R421
2007-003001	R422
2007-003025	R630
2007-007100	R205
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2007-007142	R208
2007-007308	R211
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2404-001339	C509
2404-001348	C406
2703-001512	L401
2703-001751	L405
2703-002201	C451
2703-002204	L402
2703-002624	L301
2703-002759	L403
2801-003747	OSC201
2809-001264	OSC401
2909-001225	U402
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3709-001335	CN101
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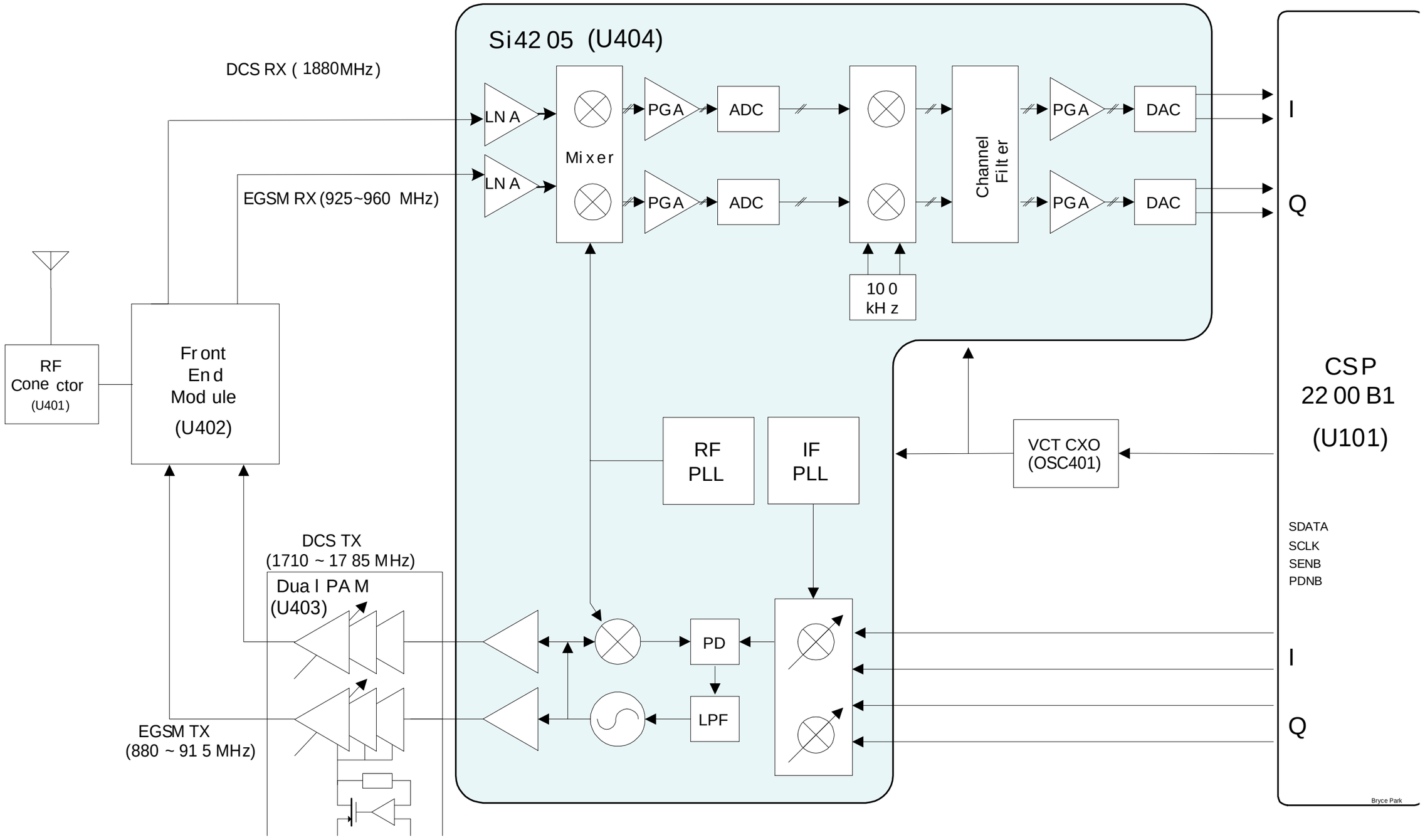
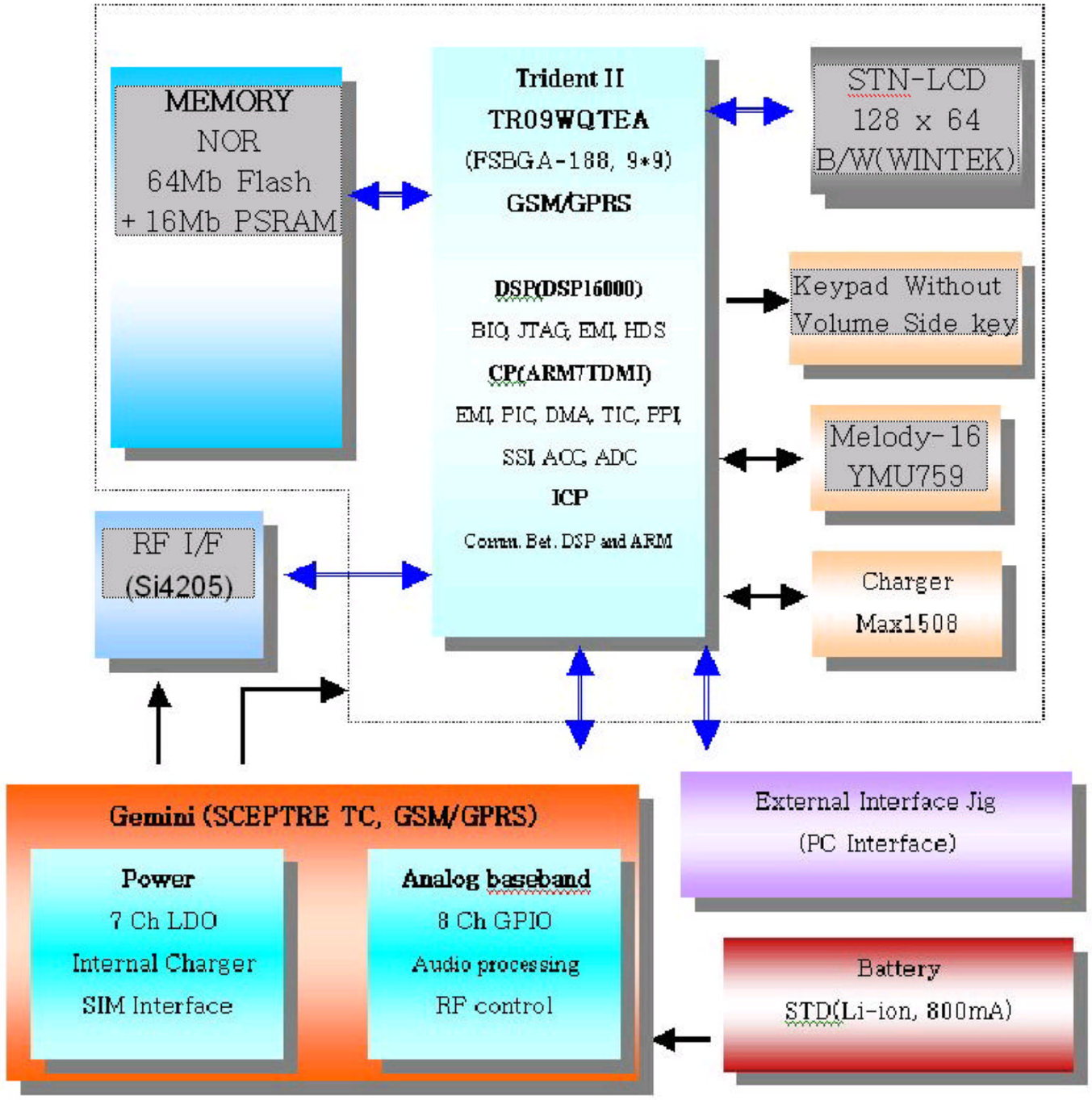
4302-001130	BAT101
GH09-00029A	U201

5. SGH-N700 Block Diagrams

1. RF Solution Block Diagram

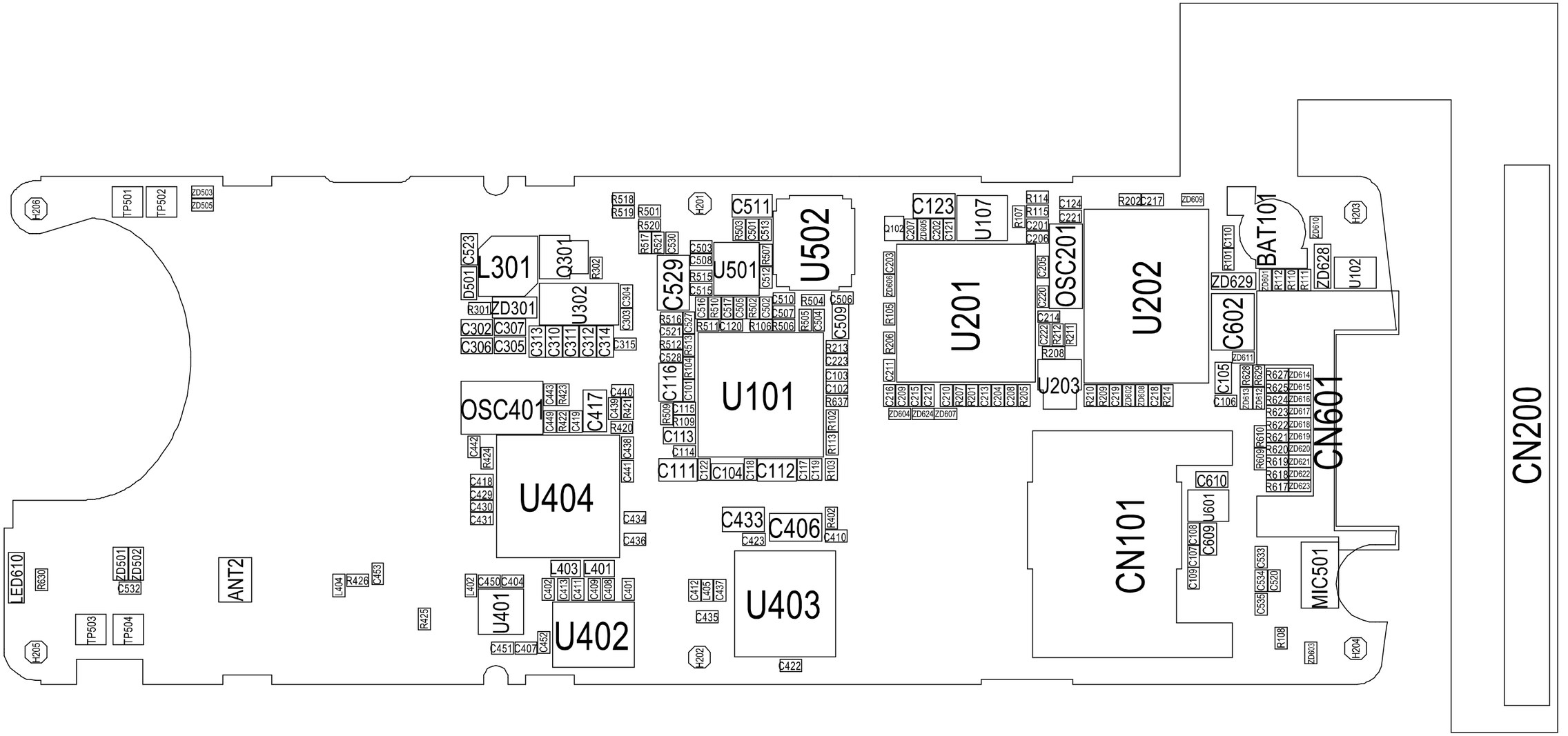


2. Base Band Solution Block Diagram

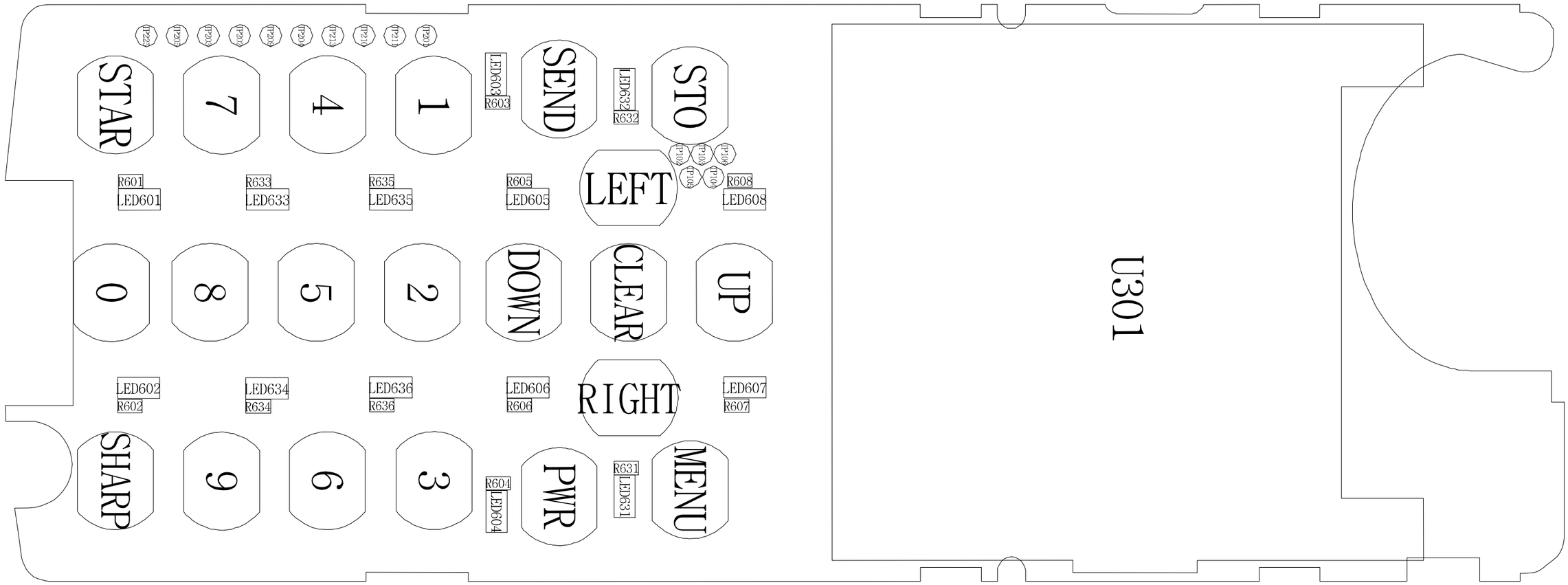


6. SGH-N700 PCB Diagrams

1. Main PCB Top Diagram

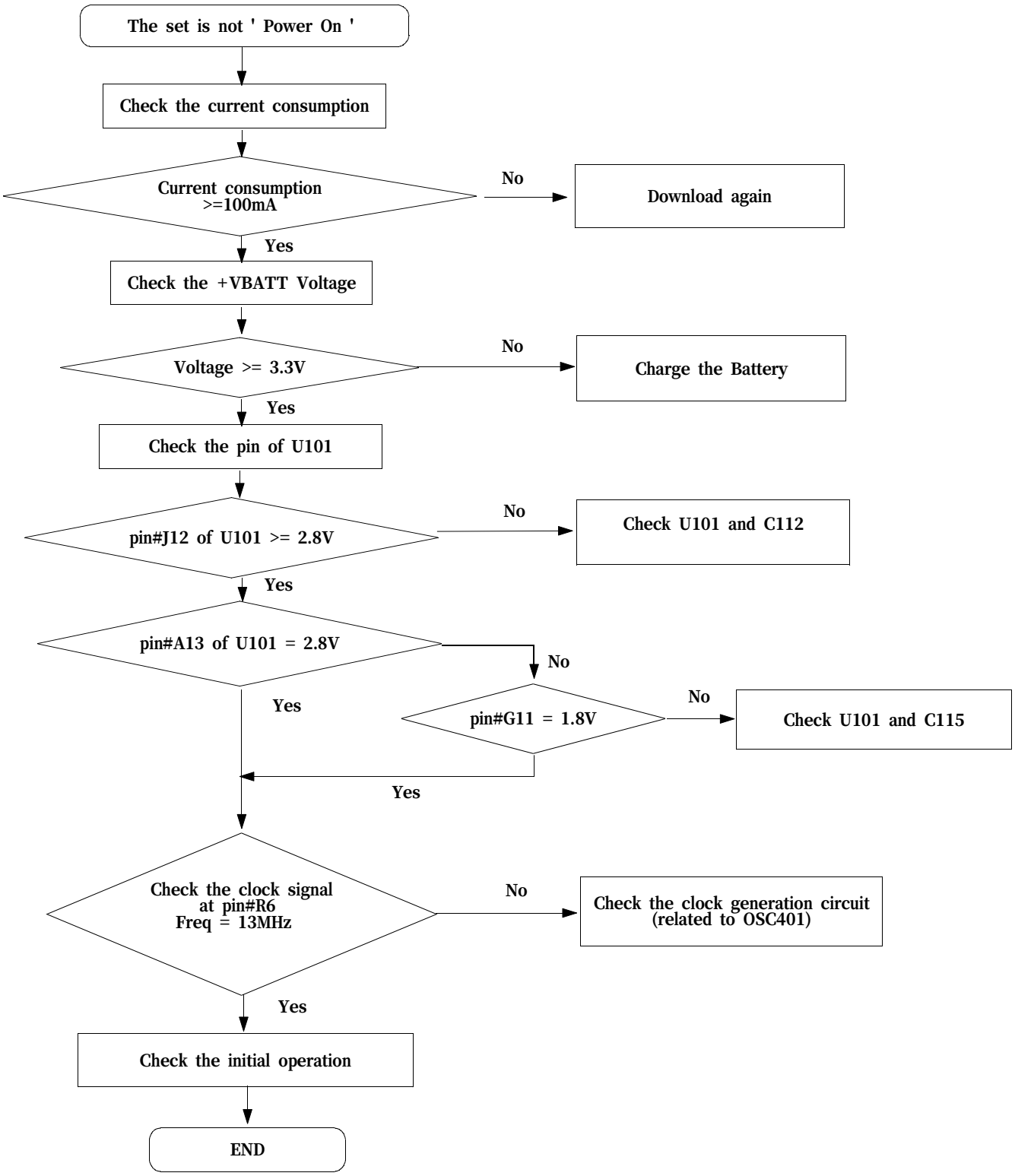


2. Main PCB Bottom Diagram

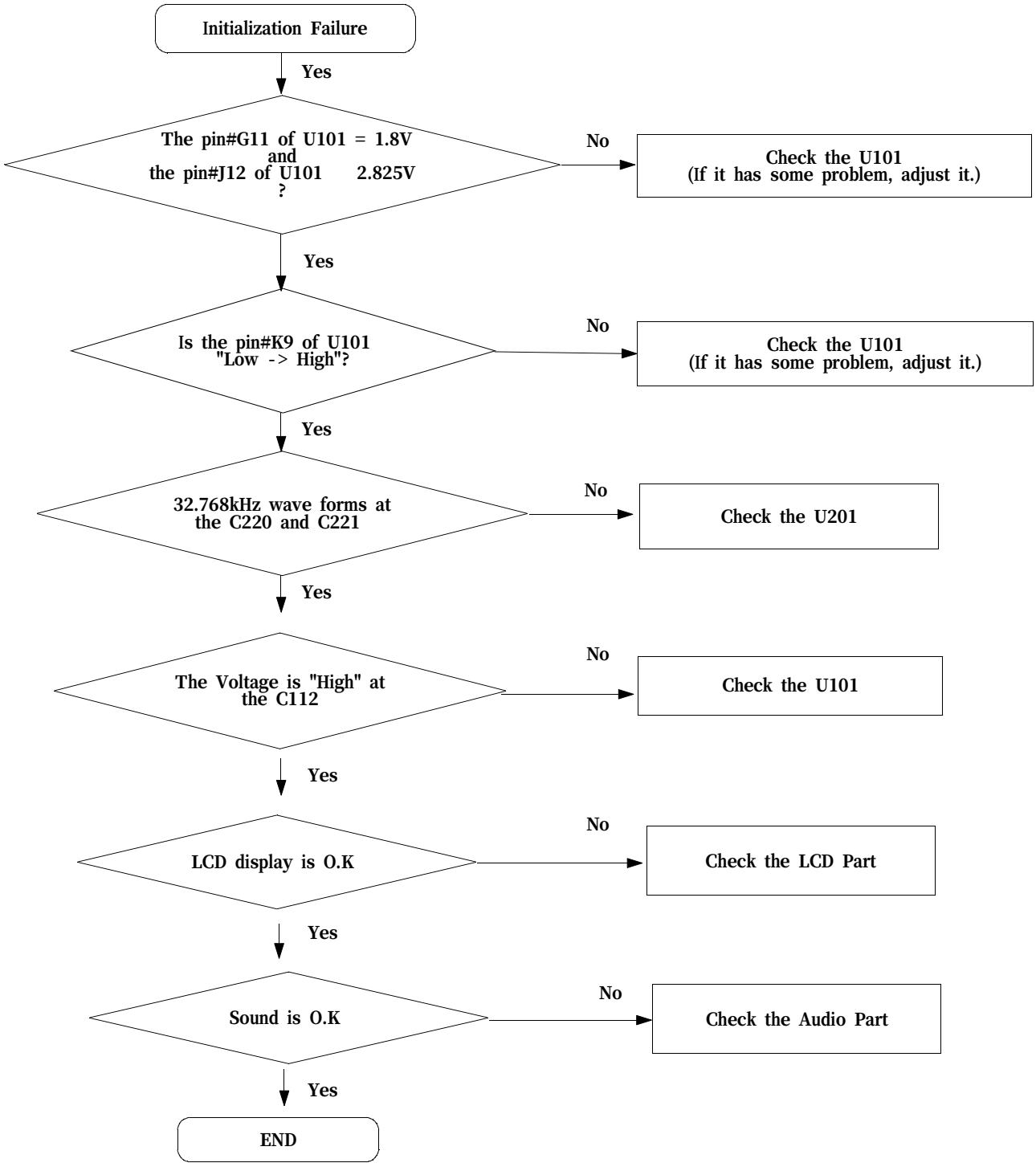


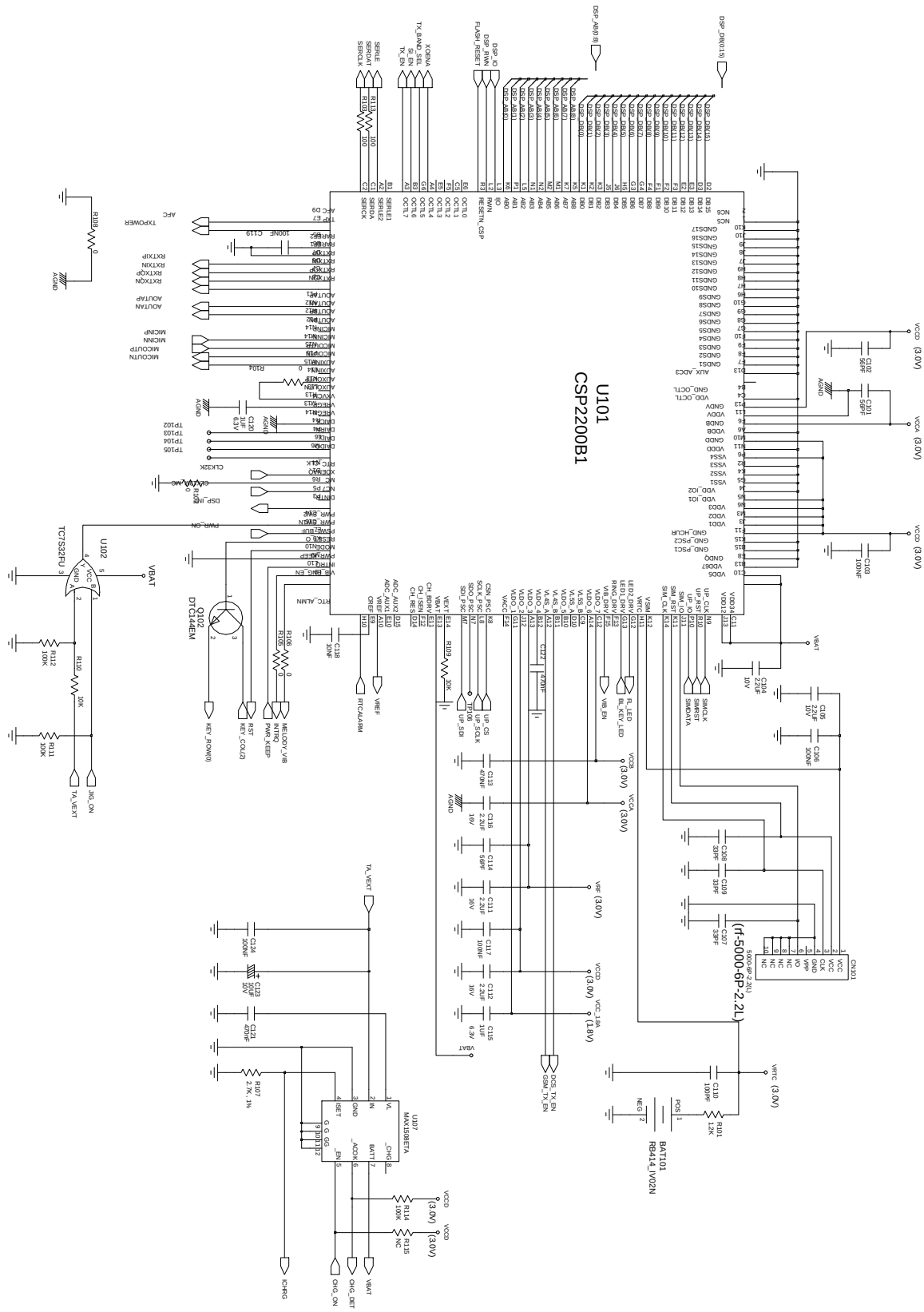
7. SGH-N700 Flow Chart of Troubleshooting

1. Power On

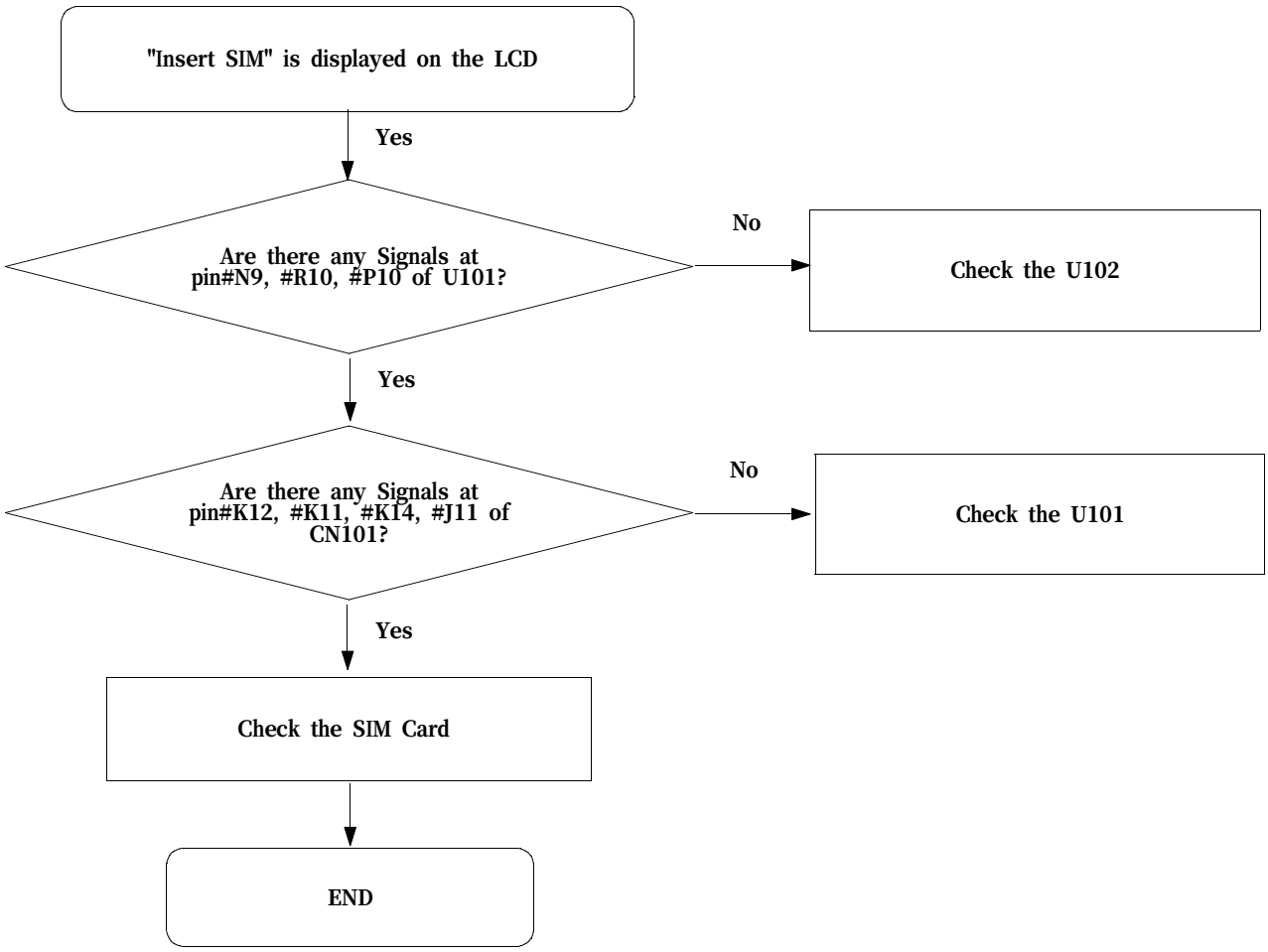


2. Initial

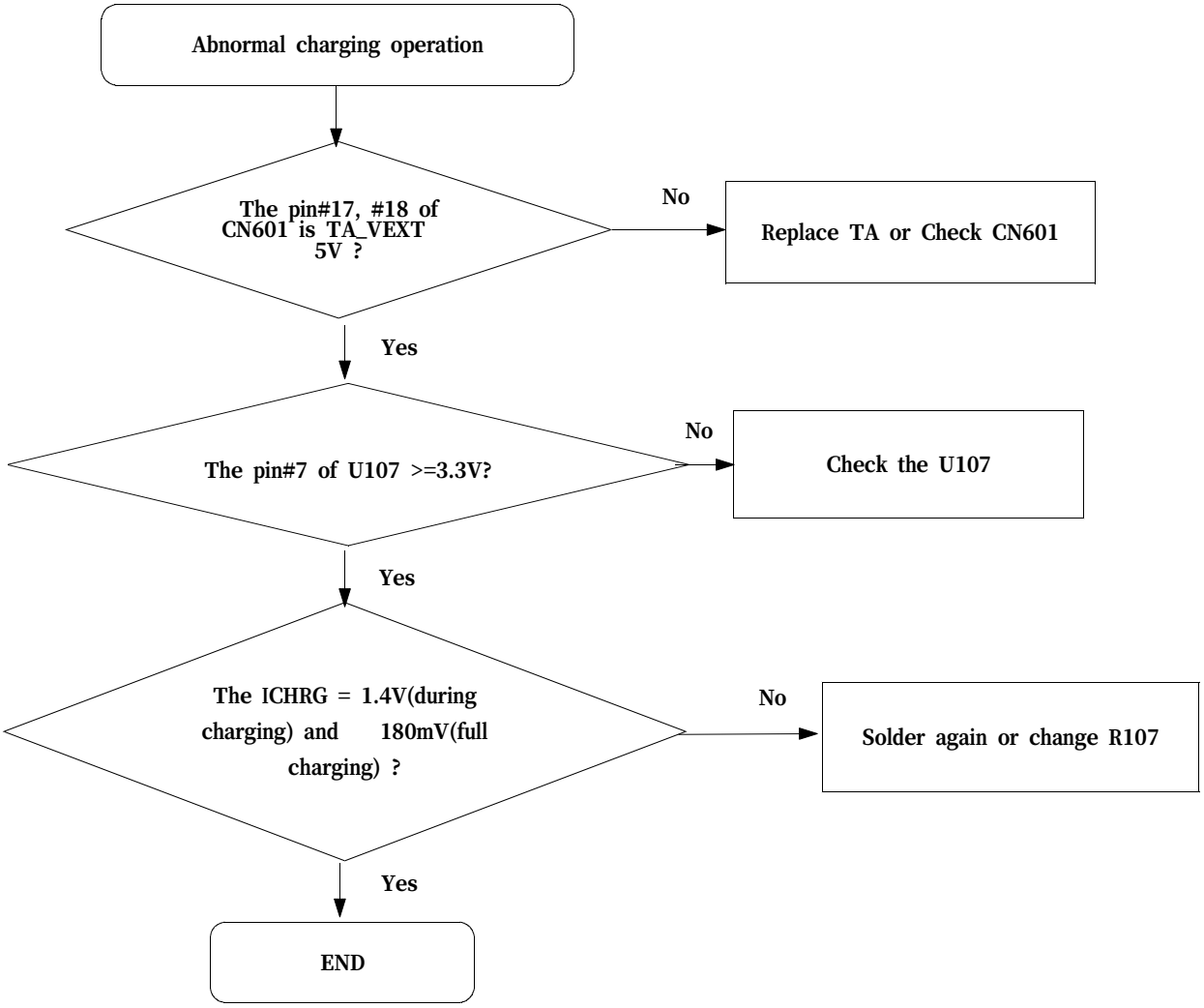


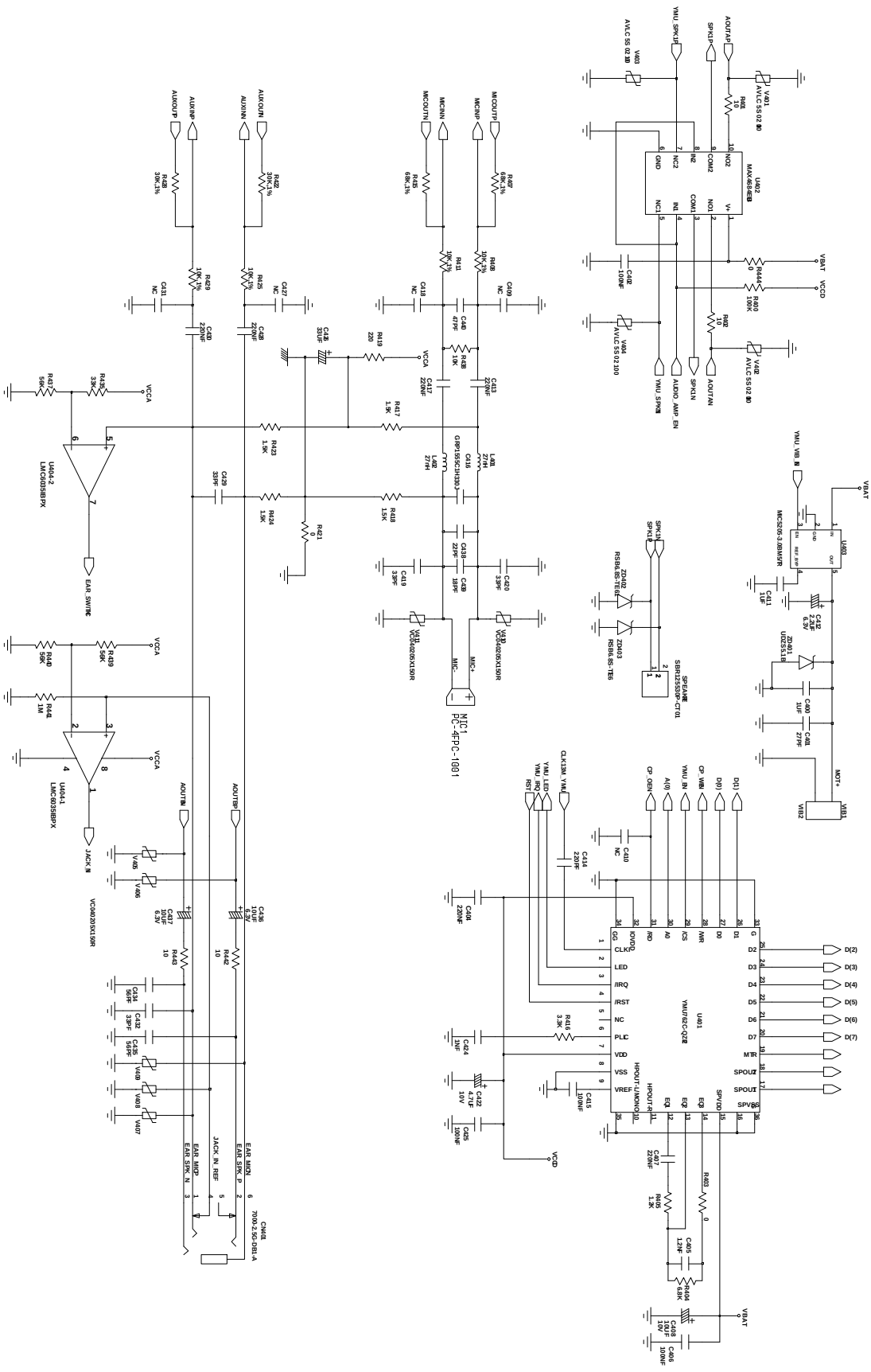


3. SIM Part

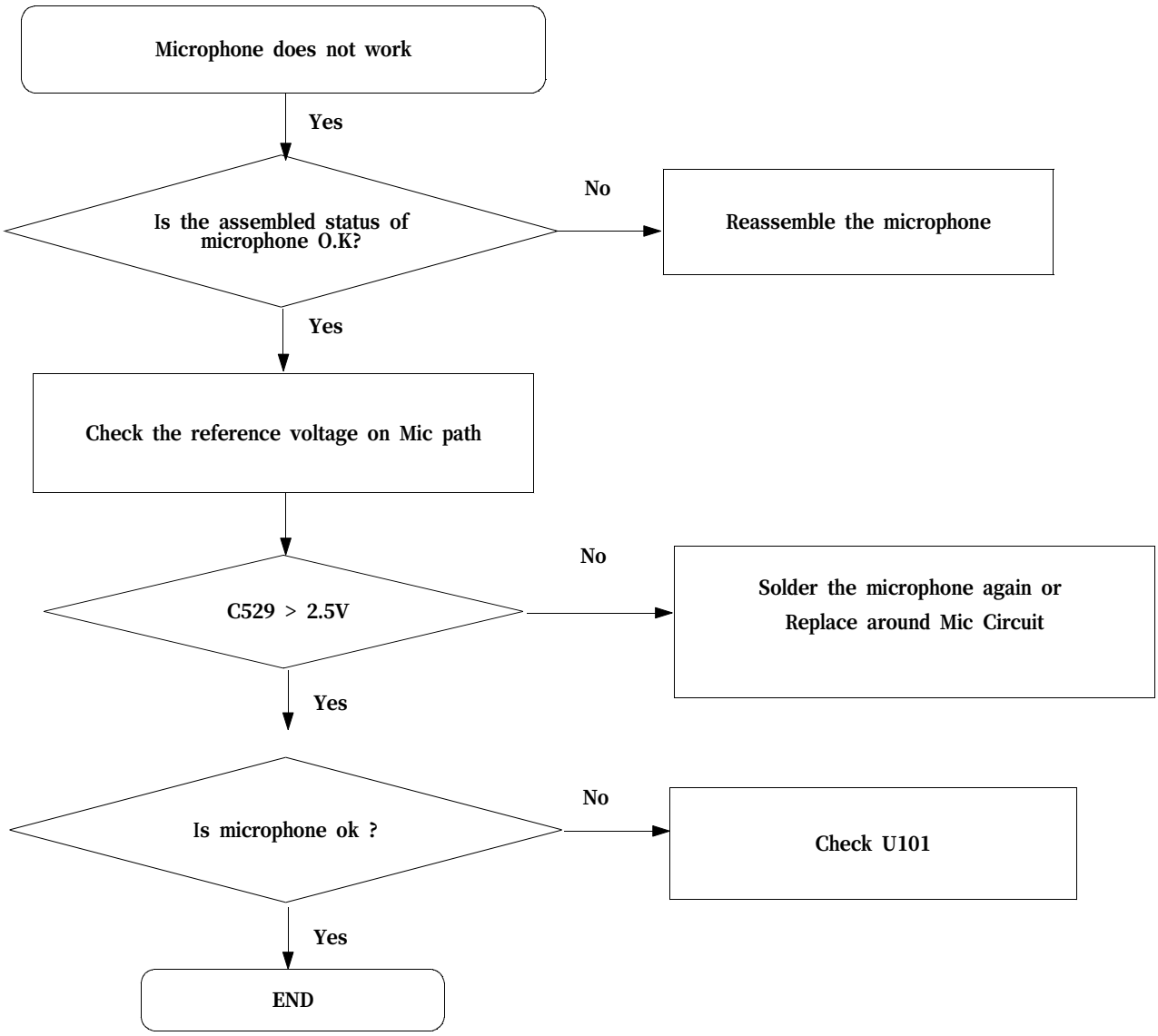


4. Charging Part

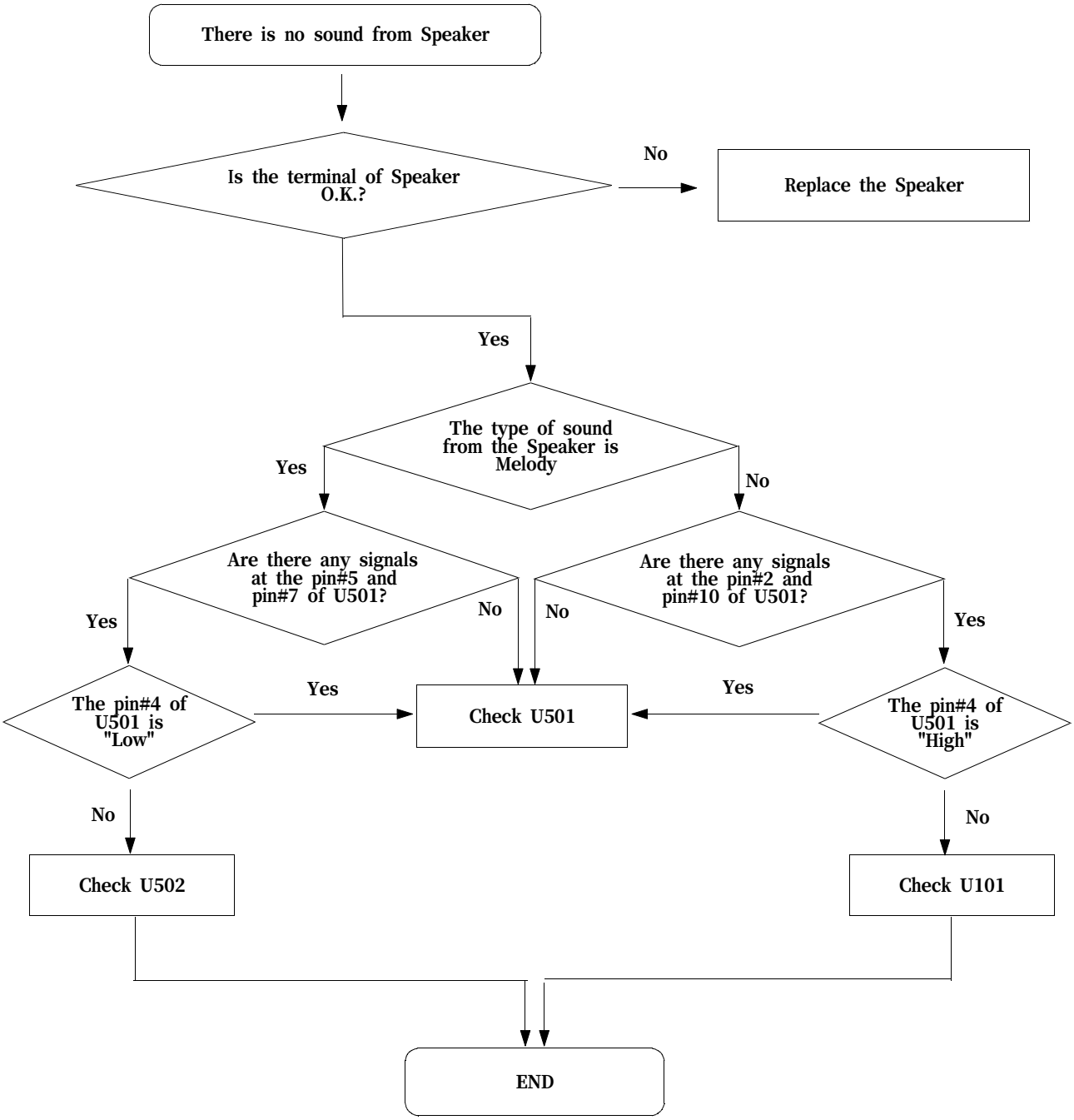


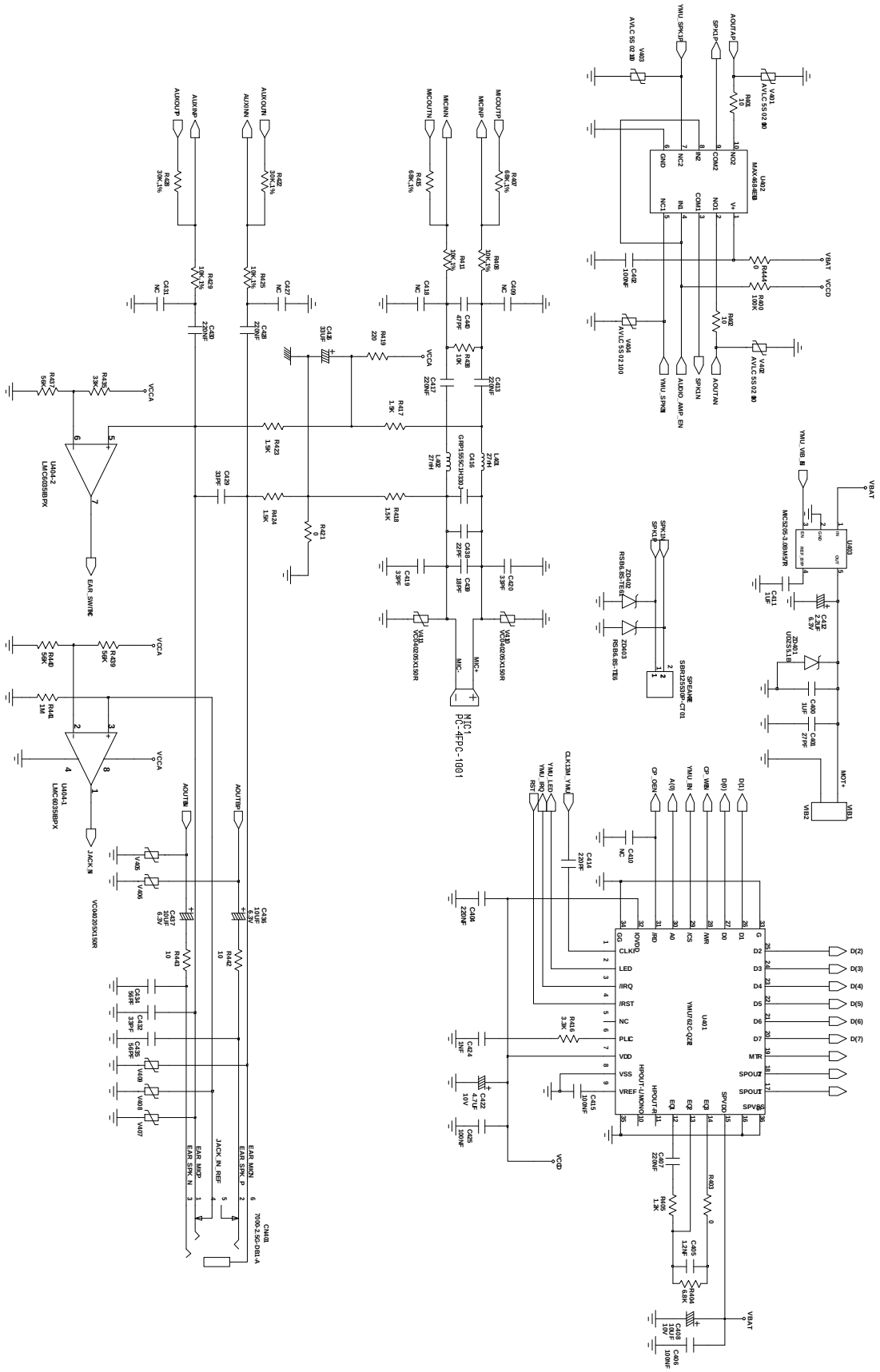


5. Microphone Part

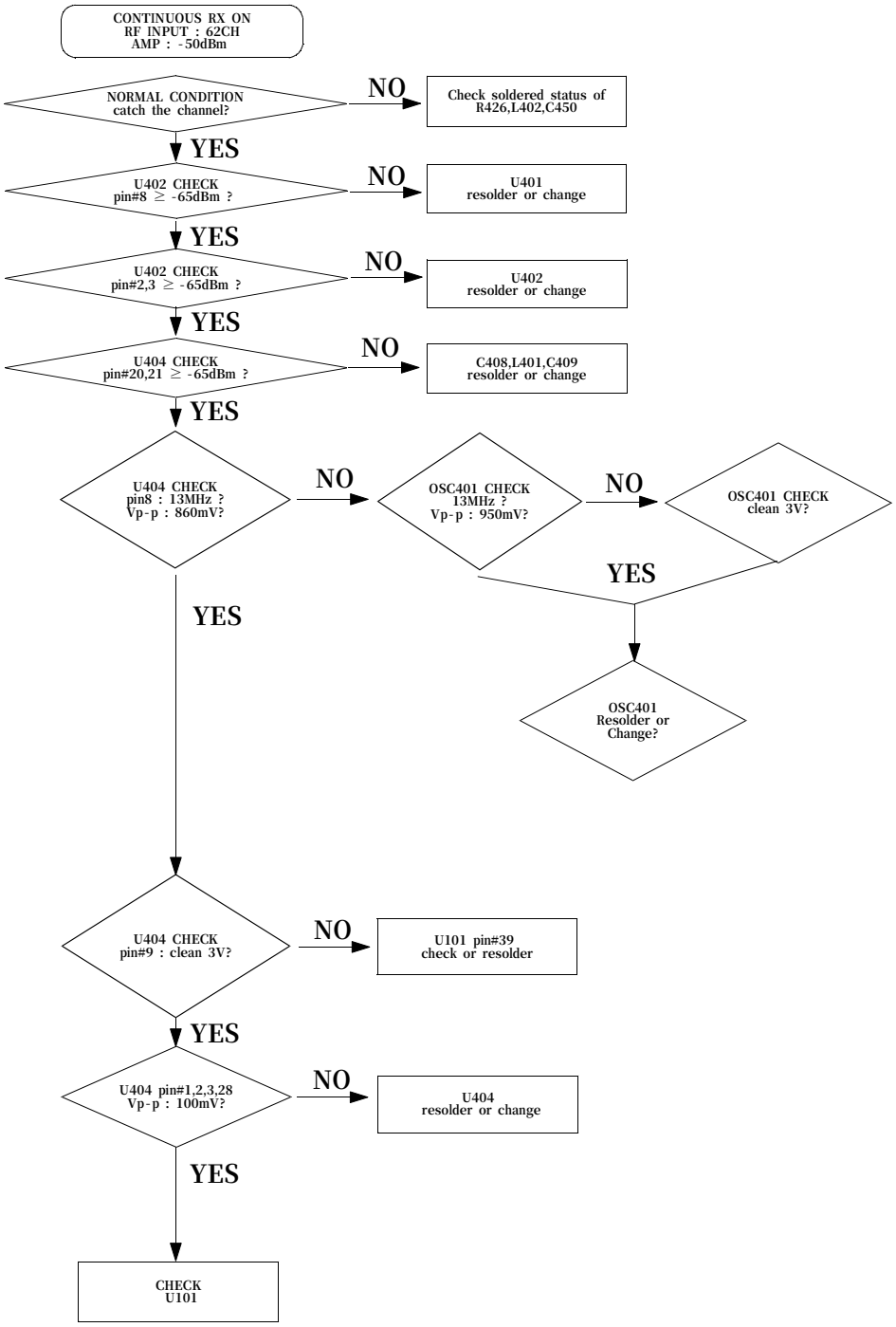


6. Speaker Part

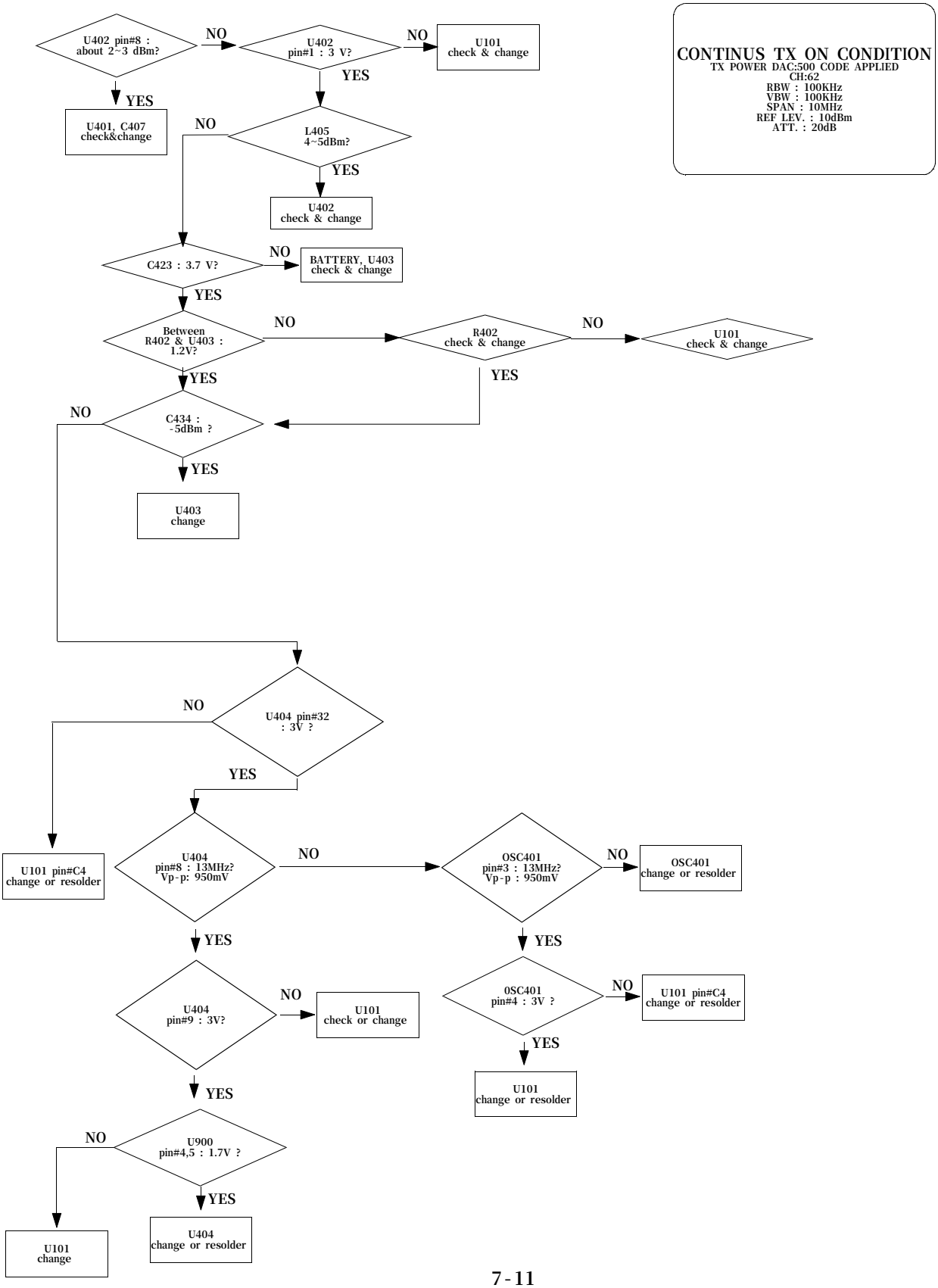




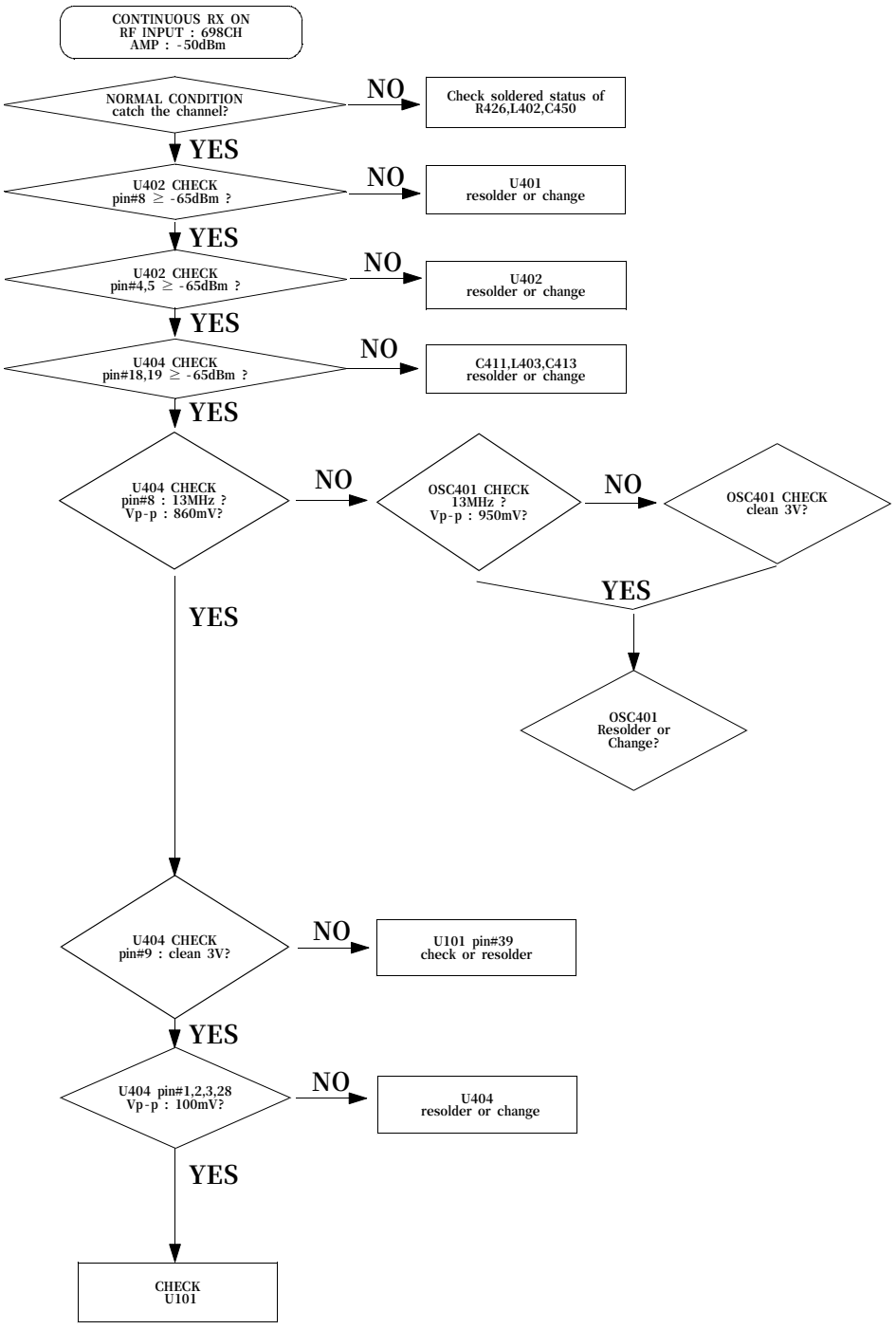
7. EGSM Reciever



8. EGSM transmitter



9. DCS Receiver



10. DCS transmitter