3. TECHNICAL BRIEF

3.1 General Description

The RF parts consists of a transmitter part, a receiver part, a synthesizer part, a voltage supply part, a VCTCXO part. And the main RF Chipset CX74017[U441]is a single-chip dual-band transceiver for the extended global system for mobile communication[E-GSM900MHz]/Digital communication system[DCS1800MHz] voice and data transfer applications.
This device integrated a direct conversion receiver architecture, which eliminates the need of Intermediate Frequency, a transmitter based on a modulation loop architecture and fractional-N synthesizer part with built in TXVCO and Local-VCO.

3.2 Receiver

The Receiver part in CX74017 contains all active circuits completely, full receiver chain with the exception of discrete front-end RF SAW filters. The filtered and amplified signal is down converted in the RF-mixer to the baseband output. The receiver path is supported by internal channel filtering. The RF front-end circuit is shown Fig. 3-1.

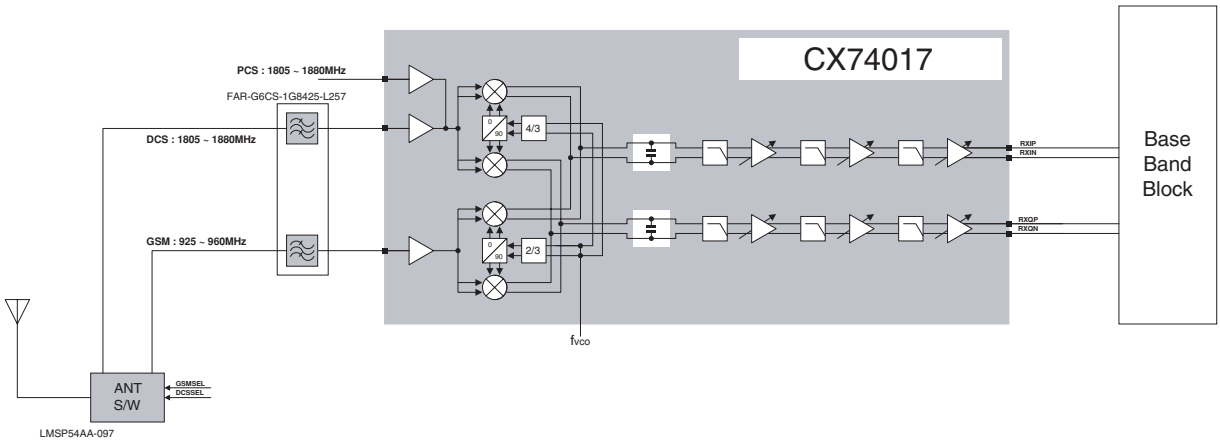


Figure 3-1. RF front-end circuit.

A. RF front end

RF front end consists of Antenna Switch(FL405), dual band LNAs integrated in transceiver(U441). The Received RF signals (GSM 925MHz ~ 960MHz, DCS 1805MHz ~ 1880MHz) are fed into the antenna or mobile switch. An antenna matching circuit is between the antenna and the mobile switch.
The Antenna Switch (FL405) is used to control the Rx and TX paths. And, the input signals VC1 and VC2 of a FL405 are connected to DCSSEL(GPO_9) and GSMSEL(GPO_11) ports of U103 to switch either TX or RX path on. When the RX path is turned on, the received RF signal then feeds either Rx_900_RF or RX_1800_RF path controlled by GSM-RX and DCS-RX respectively. This Rx_900_RF path contains one SAW filter, followed after the Antenna Switch (FL405), to filter any unwanted signal apart from the DCS RX band. And, the RX_1800_RF path is the same case.
The logic and current for Antenna Switch is given below Table 3-1.

Table 3-1. The logic and current

	VC1	VC2	Current
GSM TX	0 V	2.7 V	10.0 mA max
DCS TX	2.7 V	0 V	10.0 mA max
GSM/DCS RX	0 V	0 V	< 0.1 mA

These two paths are then connected to the LNAGSMN (#11) and LNADCSIN (#13) of CX74017 (U441), respectively. A low-noise bipolar RF amplifier, contained within the U441, amplifies the RF signal. The RF signals from the front-end pass to the receiver mixers within the U441 device.

B. Demodulator and baseband processing

In direct conversion receiver there is only one mixer down-converting received RF signal to BB signal directly. The gain down converting mixer is 40dB at high gain mode and 22dB at low gain mode.
The Rx gain setting is done in the AGC algorithm. The nominal gain of the receiver is set as a function of the expected signal strength at the antenna input so that a desired level is reached at the Rx I/Q. 7 blocks in the receiver chain have variable gains, LNA, Mixer, LPF1, VGA1, gmC Filter, Auxiliary gain control and VGA2. The gain settings can be adjustable via 3-wire bus control lines.
The baseband signals pass via integrated low-pass filters to the baseband A/D converters.
The remainder of the channel filtering is performed by the baseband chipset. The demodulator contains switches to maintain the sense of the baseband I/Q outputs with respect to the incoming RF signal on both GSM900 and DCS1800.

C. DC Offset Compensation

Three correction loops ensure that DC offsets, generated in the CX74017, do not overload the baseband chain at any point.
After compensation, the correction voltages are held on capacitors for the duration of the receive slot(s). A rising edge on the RXEN signal, selected via the serial interface, placed the DC compensation circuitry in the track mode.

3.3 Transmitter Part

The Transmitter part contains CX74017 active parts, PAM and Antenna Switch. The CX74017 active part consists of a vector modulator and offset phase-locked loop block(OPLL) including down-converter, phase detector, loop filter and dual band transmit VCO which can operate at either final RF output frequency. The RF GMSK outputs from the transmit VCO are fed directly to the RF power amplifiers.

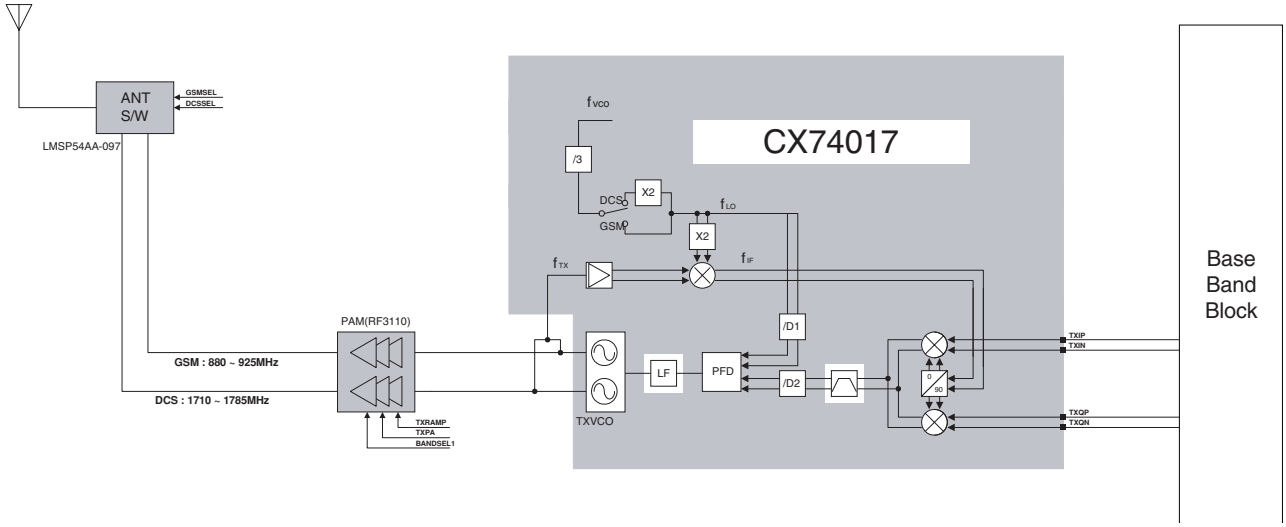


Figure 3-2. Transmitter Block diagram

The peak output power and the profile of the transmitted burst are controlled by means of power control loop. The power control function is integrated, eliminating the need for directional couplers, detector diodes, power control IC and other power control circuitry. This allows the module to be driven directly from the DAC output. The PA outputs from the directional coupler pass to the antenna connector via Antenna Switch.

A. IF Modulator

The baseband converter(BBC) within the GSM chipset generates I and Q baseband signals for the transmit vector modulator. The modulator provides more than 40dBc of carrier and unwanted side-band rejection and produces a GMSK modulated signal. The baseband software is able to cancel out differential DC offsets in the I/Q baseband signals caused by imperfections in the D/A converters.
The TX-Modulator implements a quadrature modulator. The IF-frequency input signal is split into two precise orthogonal carriers, which are multiplied by the baseband modulation signal IT/ITX and QT/QTX. It is used as reference signal for the OPLL.

B. OPLL

The offset mixer down converts the feedback Tx RF signal using LO to generate a IF modulating signal. The IF signal goes via external passive bandpass filter to one port of the phase detector. The other side of the phase detector input is LO signal. The phase detector generates an error current proportional to the phase difference between the modulated signal from the offset mixer and the reference signal from the LO.
The error current is filtered by a second order low-pass filter to generate an output voltage which depends on the GMSK modulation and the desired channel frequency. This voltage controls the transmit VCO such that the VCO output signal, centered on the correct RF channel, is frequency modulated with the original GMSK data. The OPLL acts as a tracking narrowband band pass filter tuned to the desired channel frequency. This reduces the wideband noise floor of the modulation and up-conversion process and provides significant filtering of spurious products.

C. Synthesizer

The CX74017 includes a fully integrated UHF VCO with an on-chip LC tank.
A single sigma-delta fractional-N synthesizer can phase lock the local osillator used in both transmit and receive path to a precision frequency reference input. Fractional-N operation offers low phase noise and fast setting times, allowing for multiple slot applications such as GPRS.
The generated frequency is given by the following equation

$$f_{VCO} = \frac{\left(N + 3.5 + \frac{FN}{2^{22}}\right) f_{ref}}{R}$$

where : f_{VCO} = Generated VCO frequency

N = N-divider ratio integer part

FN = Fractional setting

R = R-divider ratio

f_{VCO} = Reference Frequency

The counter and mode settings of the synthesizer are also programmed via 3-wire interface.

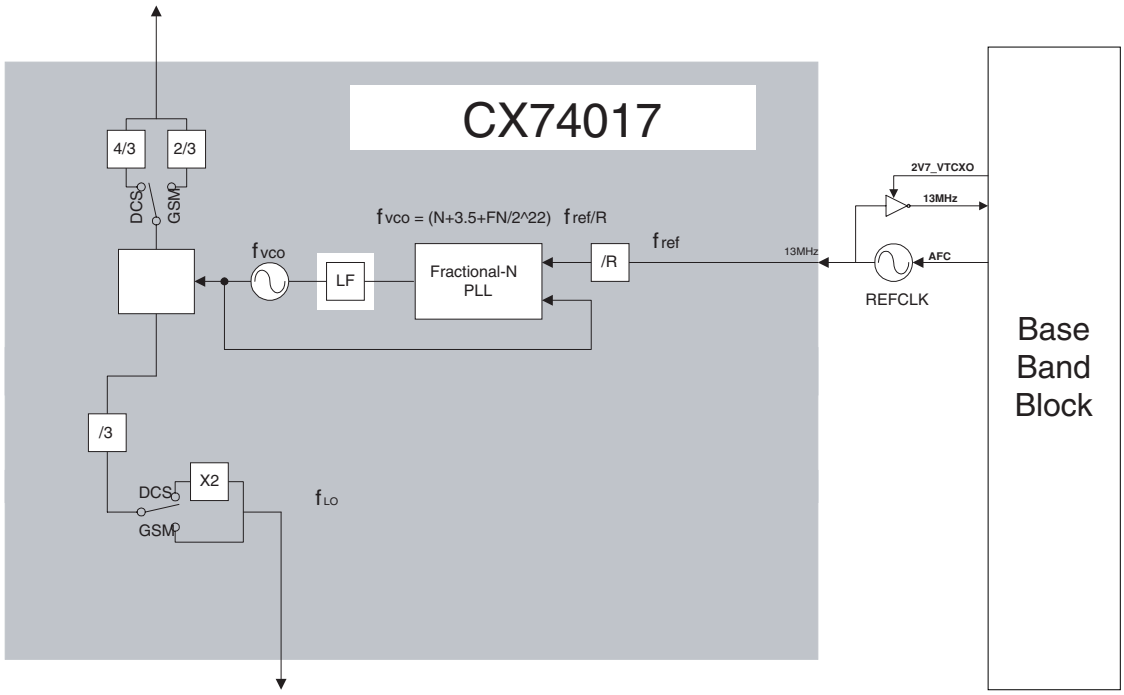


Figure 3-3. Synthesizer Block diagram

D. Power Amplifier

The RF3110[U416] is a Dual band amplifier for E-GSM(880 to 915MHz) and DCS1800(1710 to 1785MHz). The efficiency of module is the 50% at nominal output power for E-GSM and the 45% for DCS1800. This module should be operated under the GSM burst pulse. To avoid permanent degradation, CW operation should not be applied. To avoid the oscillation at no input power, before the input is cut off, the control voltage Vapc should be control to less than 0.5V.
We have to improve thermal resistance, the through holes should be layouted as many as possible on PCB under the module. And to get good stability, all the GND terminals should be soldered to ground plane of PCB.

3.4 13 MHz Clock

The 13 MHz clock (VC-TCXO-208C) consists of a TCXO (Temperature Compensated Crystal Oscillator) which oscillates at a frequency of 13 MHz.
It is used within the CX74017 RF Main Chip, BB Analog chip-set (AD6521), and Digital (AD6522).

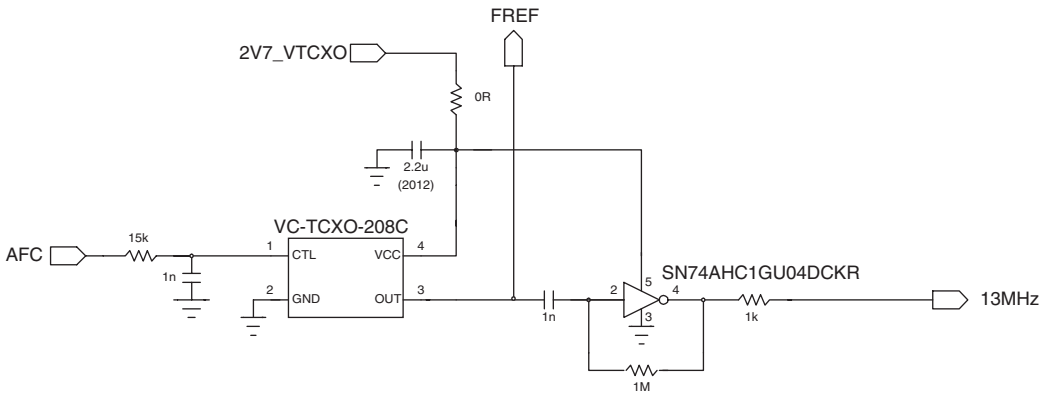


Figure 3-4. VCTCXO Circuit.

3.5 Power Supplies and Control Signals

There are two regulators used in the phone to provide RF power. One is contained inside of ADP3408 (U101), power management IC to provide the power for the VCTXO (X401). The other is used to provide the power for remaining RF circuits.

Table 3-2.

Regulator	Voltage	Powers	Enable Signal
Regulator 1 (U101, 2V7_VTCXO)	2.7 V ± 0.5 V	VCTXO	
Regulator 2 (U414, RF2V8)	2.85 V ± 0.5 V	RF circuitry	VSYNTHEN

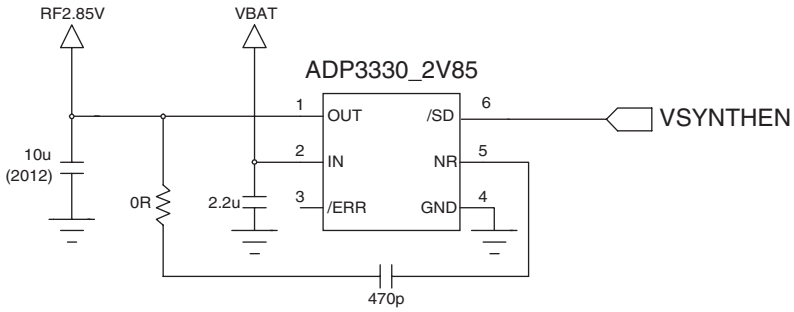


Figure 3-5. Regulator Circuit.

3.6 Testing Set-up and Checking Signals

A. Received RF Level and Checks

This section shows the typical RF levels expected throughout the receiver path. A block diagram showing the locations of the RF measurement points and levels is shown in Fig. 3-11.

Receiver Testing Set-up

To check the receiver the following conditions have to be set:

On a signal generator or a GSM/DCS test box, output a CW signal of amplitude = -60 dBm at either: 947.4 MHz (CH62) when testing the GSM RX path or 1842. 6 MHz (CH699) when testing the DCS RX path. Set the DC power supply to 4.0 V.

Note: All RF values shown are only intended as a guide figure and may differ from readings taken with other test equipment and leads. Lead and connector losses should always be taken into account when performing such RF measurements.

Testing Receiver

Using a suitable high frequency probe measure the RF levels at the relevant points shown in Fig. 3-9 and compare your measurements with those shown in the diagram. If there are any major difference between the readings taken and those indicated then further investigation of that particular point will be required. It will also be necessary to ensure that all the following power supplies and signals are present which control this part of the receiver circuit :

1. The Control Signal of FEM (see Fig. 3-15, 16, 17)
2. RF2V8 (see Fig. 3-12)
3. 2V7_VTCXO (see Fig. 3-13)
4. 13MHz(see Fig. 3-14)
5. CLK, DATA, SEN (see Fig. 3-18)
8. RX IP, IN, QP, QN (see Fig. 3-21)

B. Transmitted RF Level and Checks

This section shows the typical RF levels expected throughout the transmitter path. A block diagram showing the locations of the RF measurement points and levels is shown in Fig. 3-8.

Transmitter Testing Set-up

To check the transmitter the following conditions have to be set :

1. Set the DC Power supply to 4.0 V.
2. Power up the GSM/DCS test set and then establishing a call with an attached mobile on active mode.
3. Select Channel, TX Level and Input Level according to which parameter is required.

Note: All RF values shown are only intended as a guide figure and may differ from readings taken with other test equipment and leads. Lead and connector losses should always be taken into account when performing such RF measurements.

Testing Transmitter

Using a suitable high frequency probe measure the RF levels at the relevant points shown in Fig. 3-9, 10. and compare your measurements with those shown in the diagram. If there are any major difference between the readings taken and those indicated then further investigation of that particular point will be required. It will also be necessary to ensure that all the following power supplies and signals are present which control this part of the transmitter circuit:

1. The Control Signal of FEM (see Fig. 3-15, 16, 17)
2. RF2V8 (see Fig. 3-12)
3. 2V7_VTCXO (see Fig. 3-13)
4. 13 MHz (see Fig. 3-14)
5. TXEN, TXRAMP, TXPA (see Fig. 3-19)
6. TX IP, IN, QP, QN (see Fig. 3-20)

RF components (Component Side)

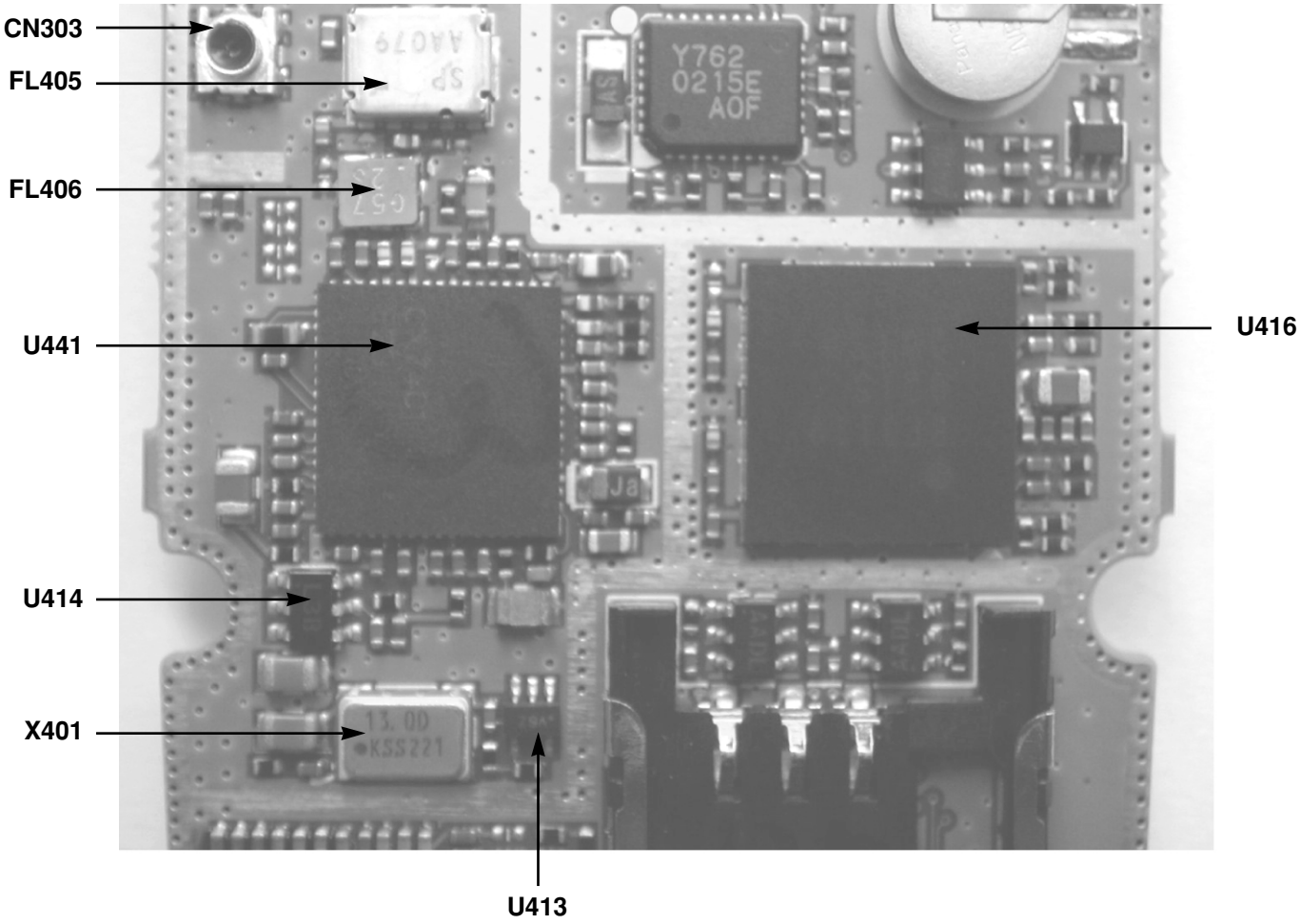


Figure 3-6. RF components (Component Side).

Reference	Description	Reference	Description
U441	RF Main Chipset	FL406	Dual SAW Filter
CN303	Mobile S/W	X401	VCTCXO
FL405	Ant. S/W	U414	LDO
U416	PAM	U413	Inverter IC

Test point of Rx Levels

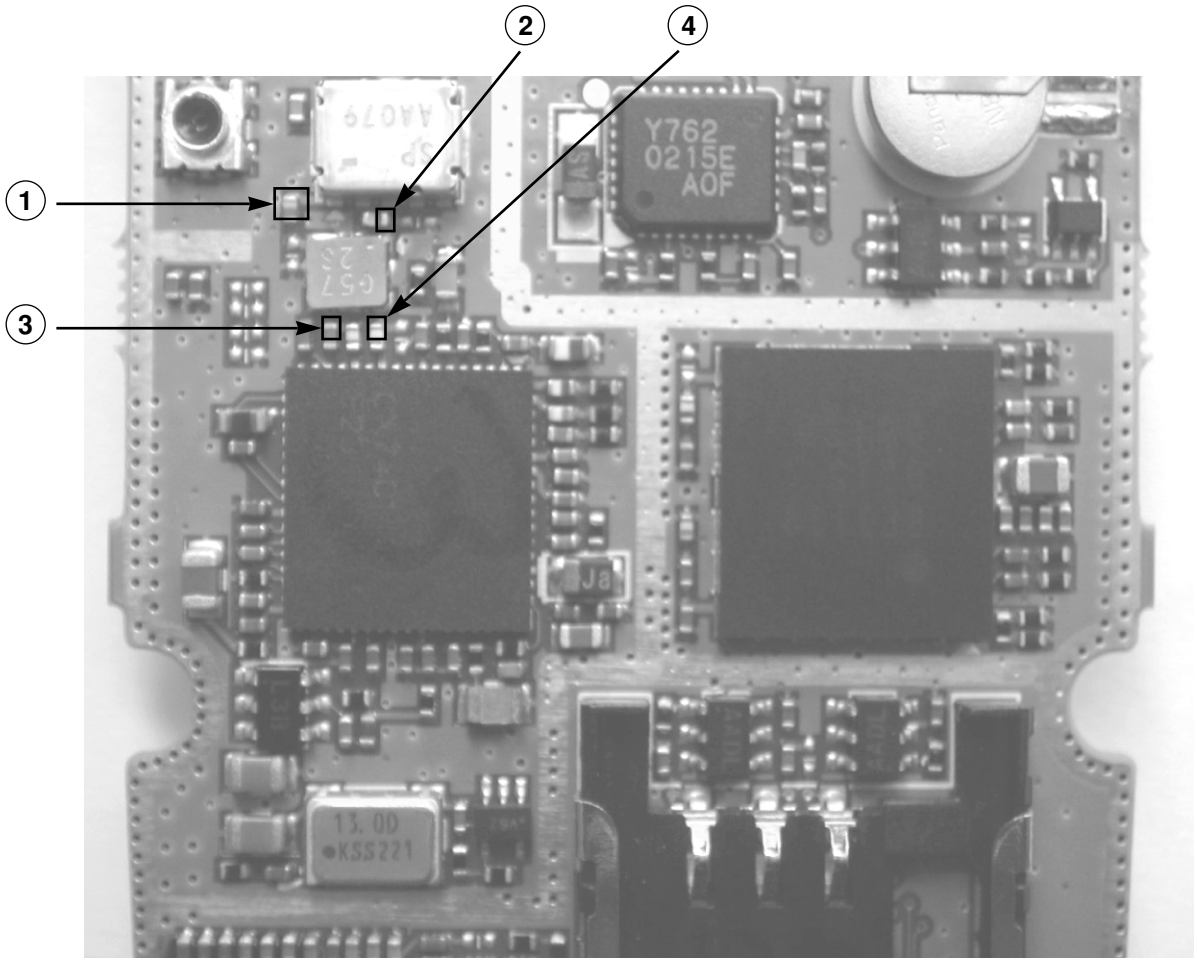


Figure 3-7. Test point of Rx Levels.

Test point of TX Levels

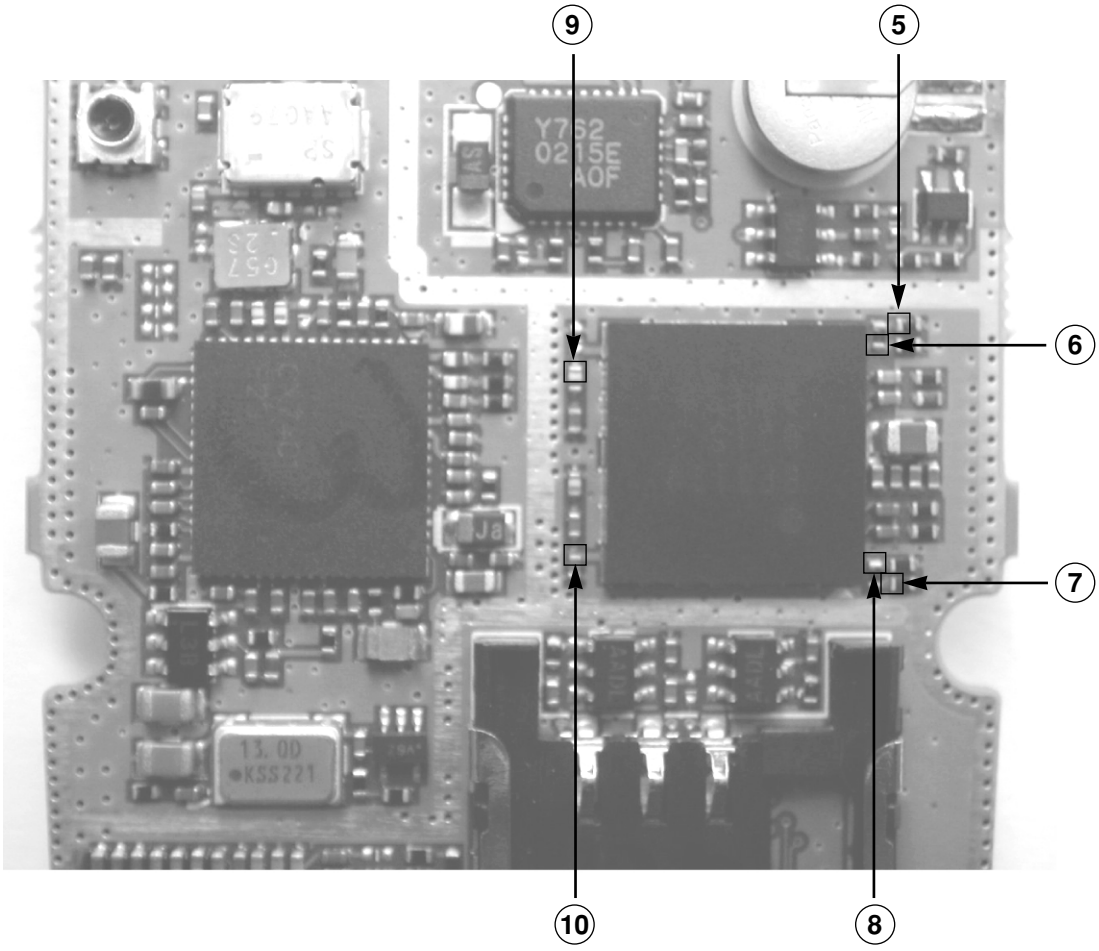


Figure 3-8. Test point of TX Levels(1).

Control signal test points (1)

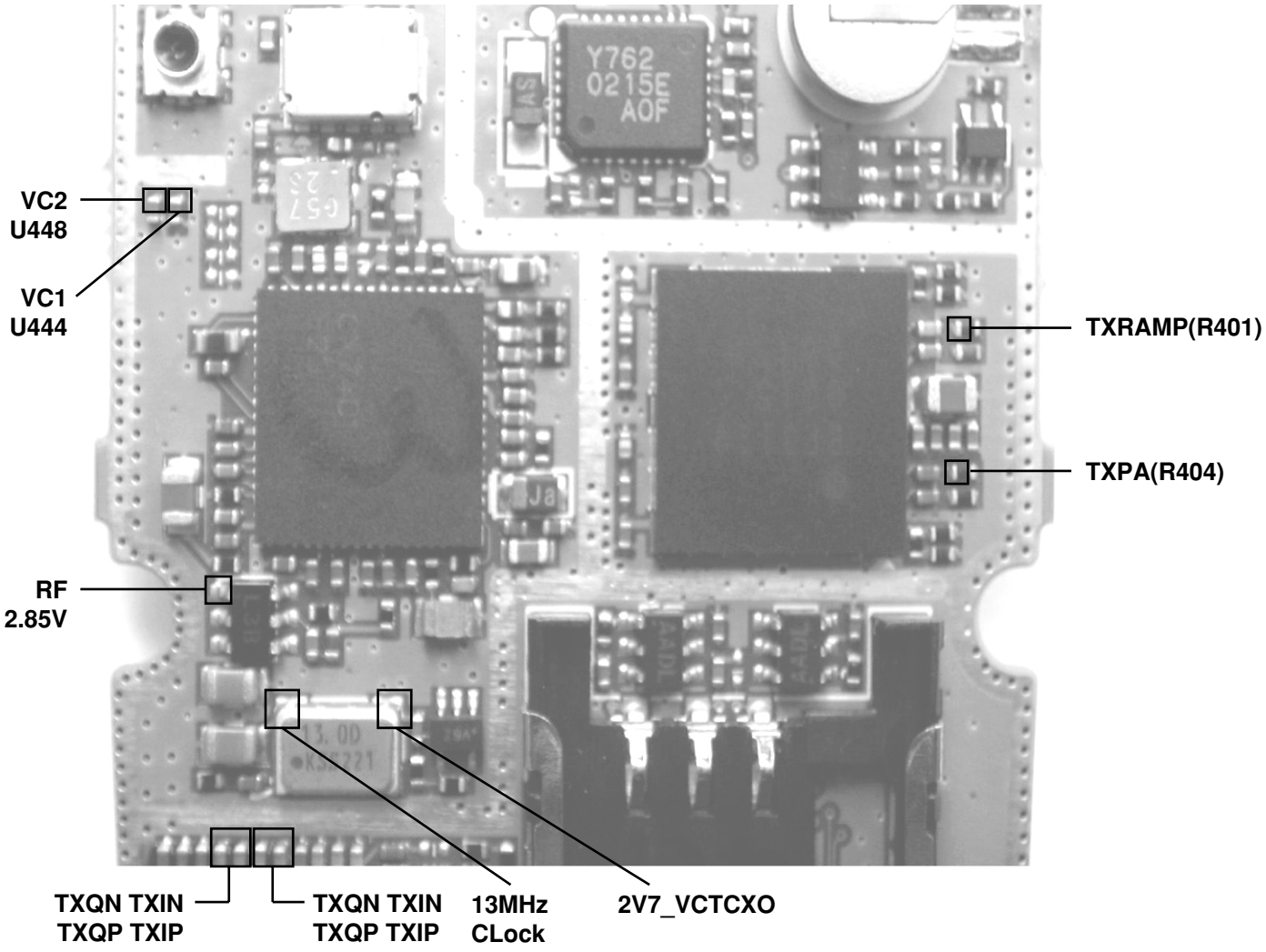


Figure 3-9. Control signal test points (1).

Control signal test points (2)

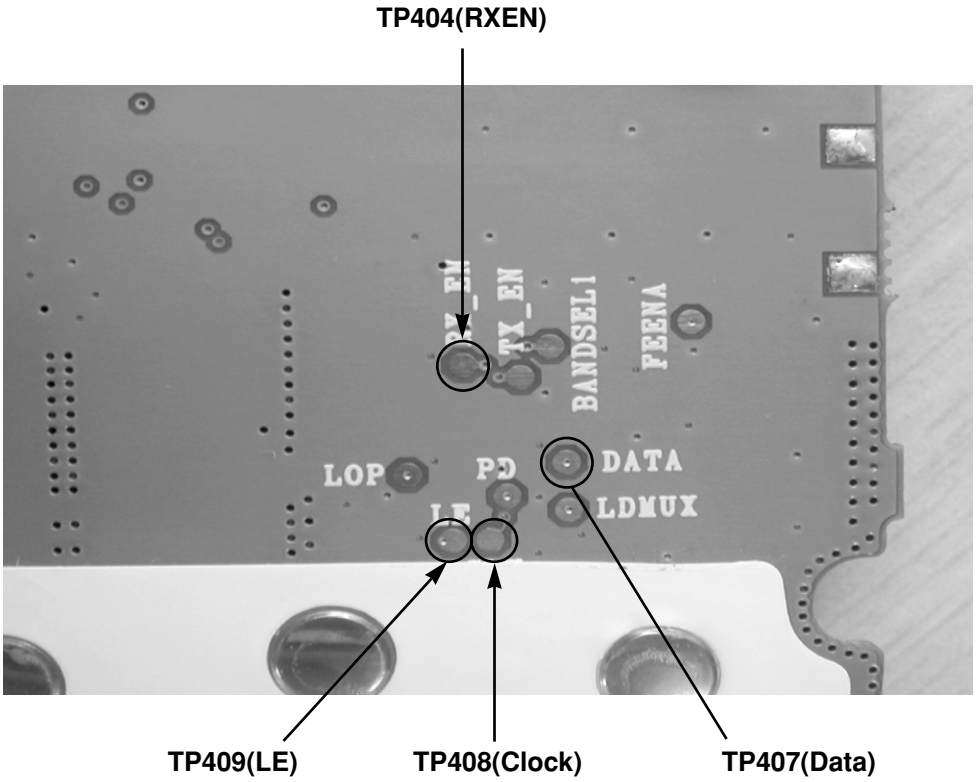


Figure 3-10. Control signal test points (2).

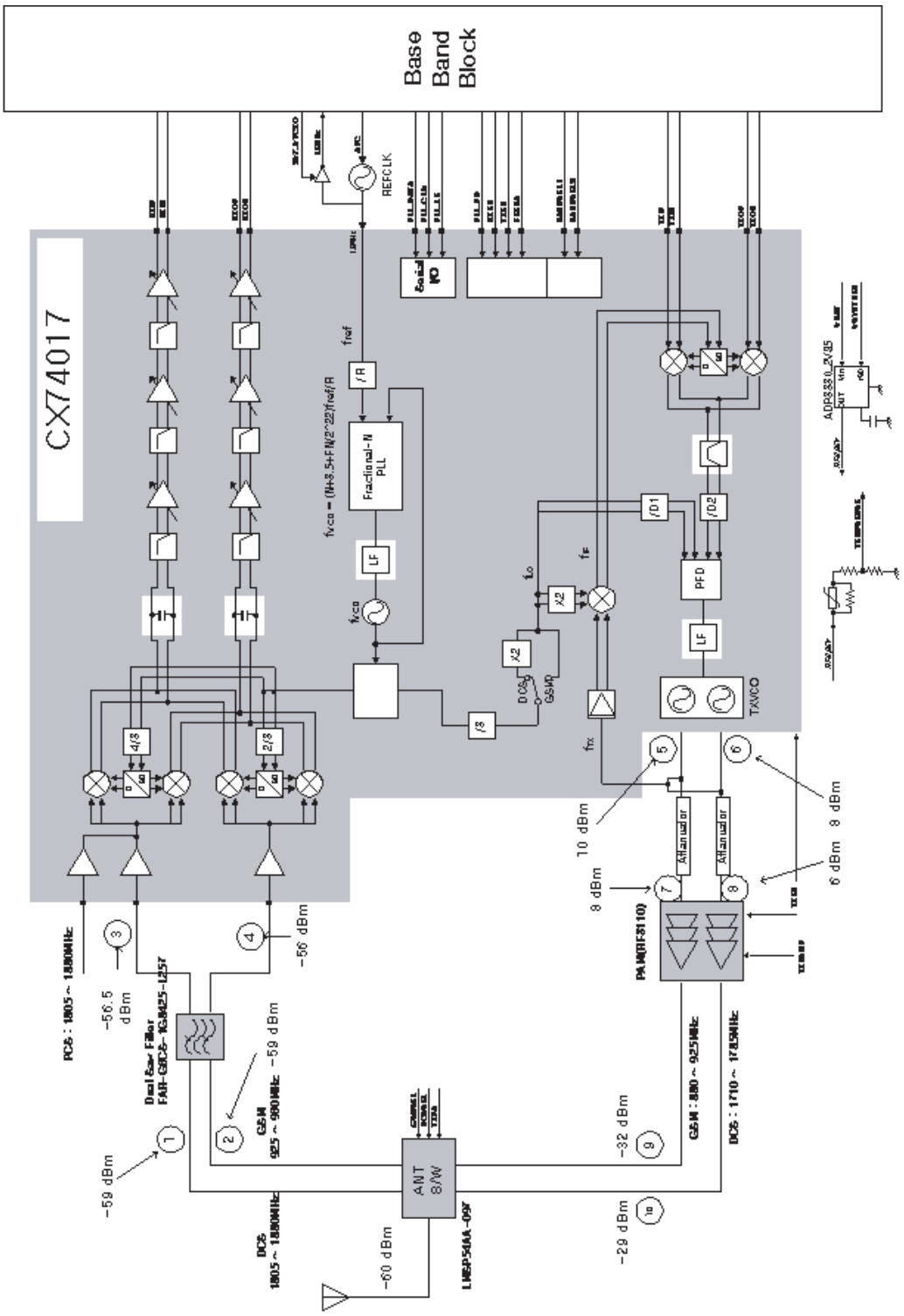


Figure 3-11. Transmitter & Receiver RF Levels

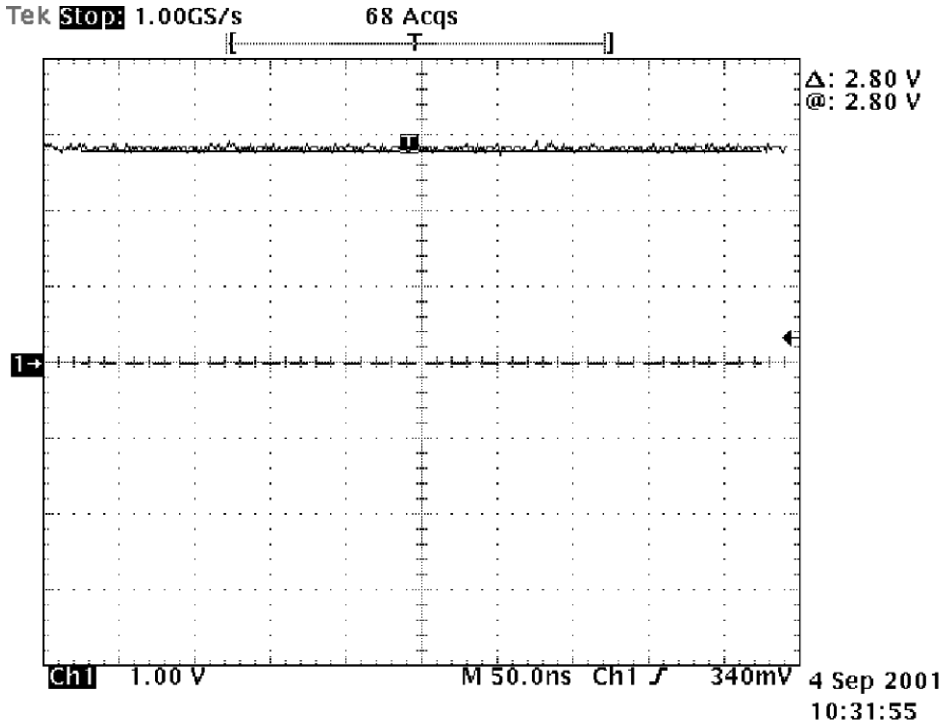


Figure 3-12. Regulator Output (RF2V8).

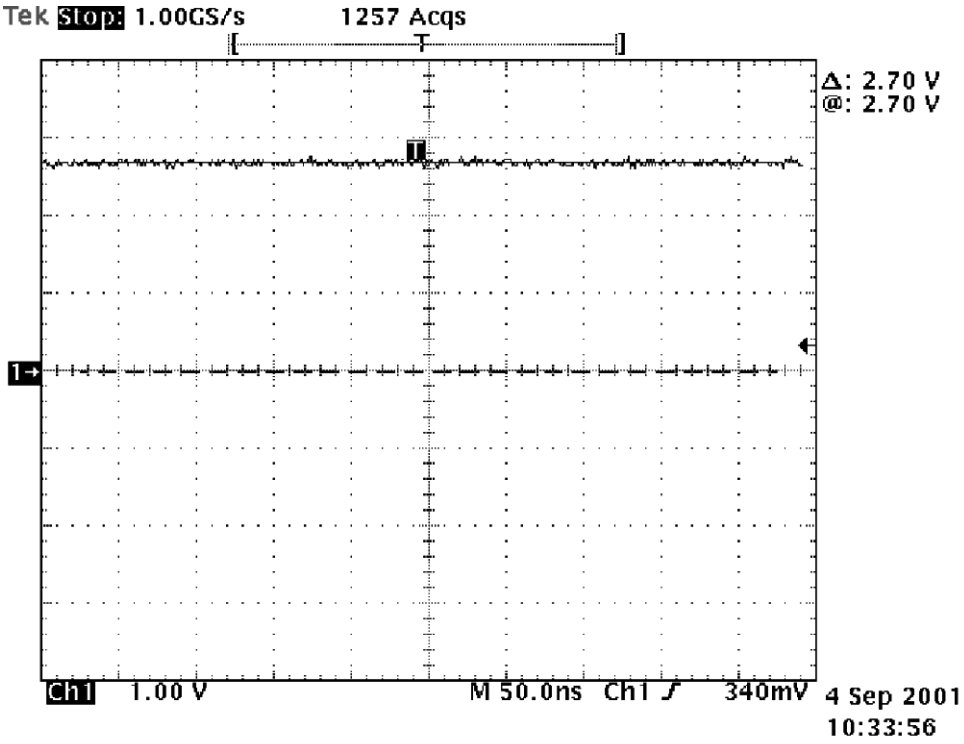


Figure 3-13. VCTCXO Power Supply (2V7_VTCXO).

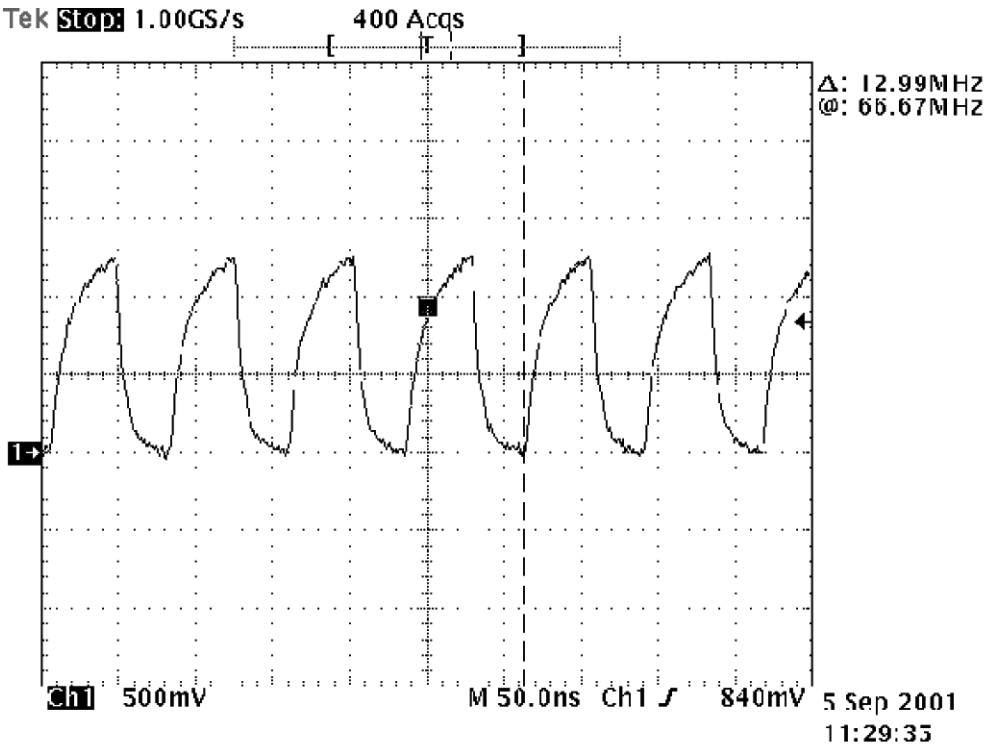


Figure 3-14. 13MHz Clock.

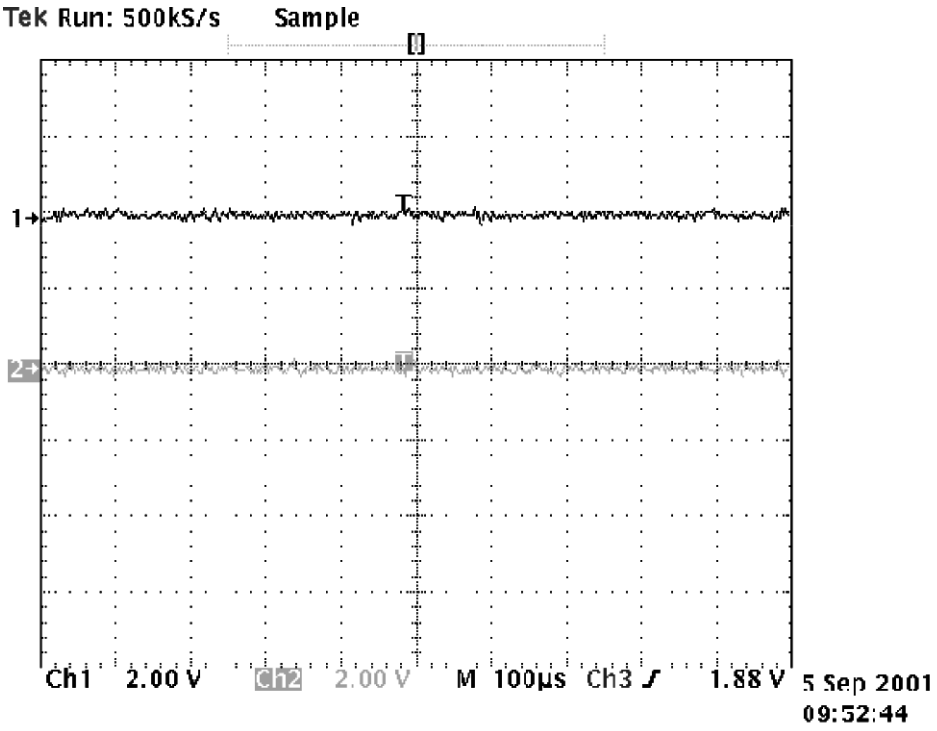


Figure 3-15. Control Signal of FEM in Rx mode (GSM,DCS both).

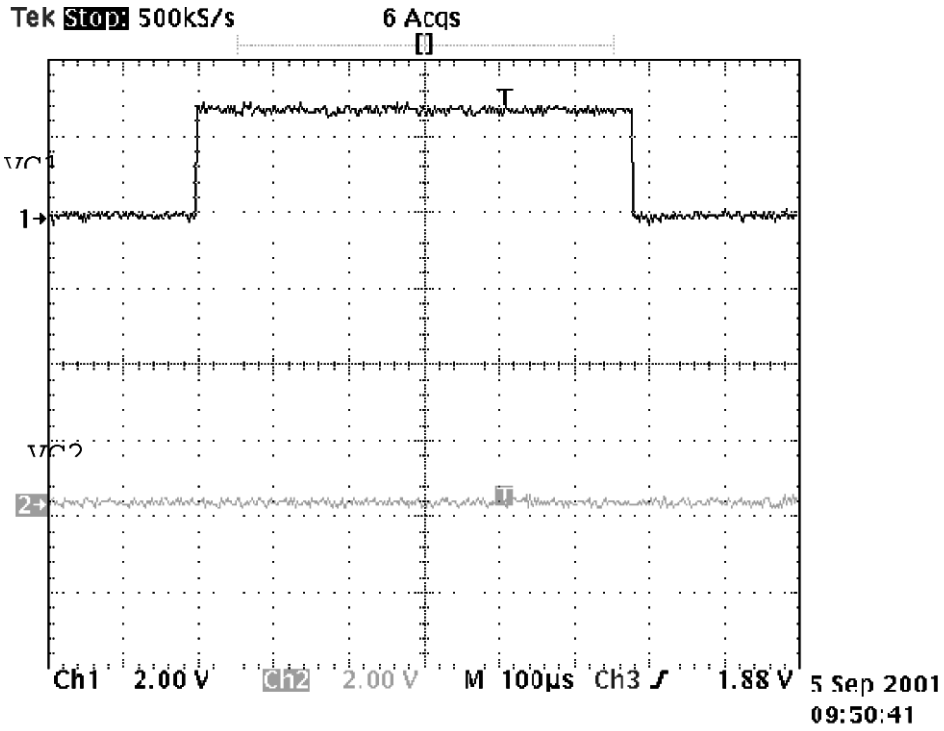


Figure 3-16. Control Signal of FEM in GSM TX mode.

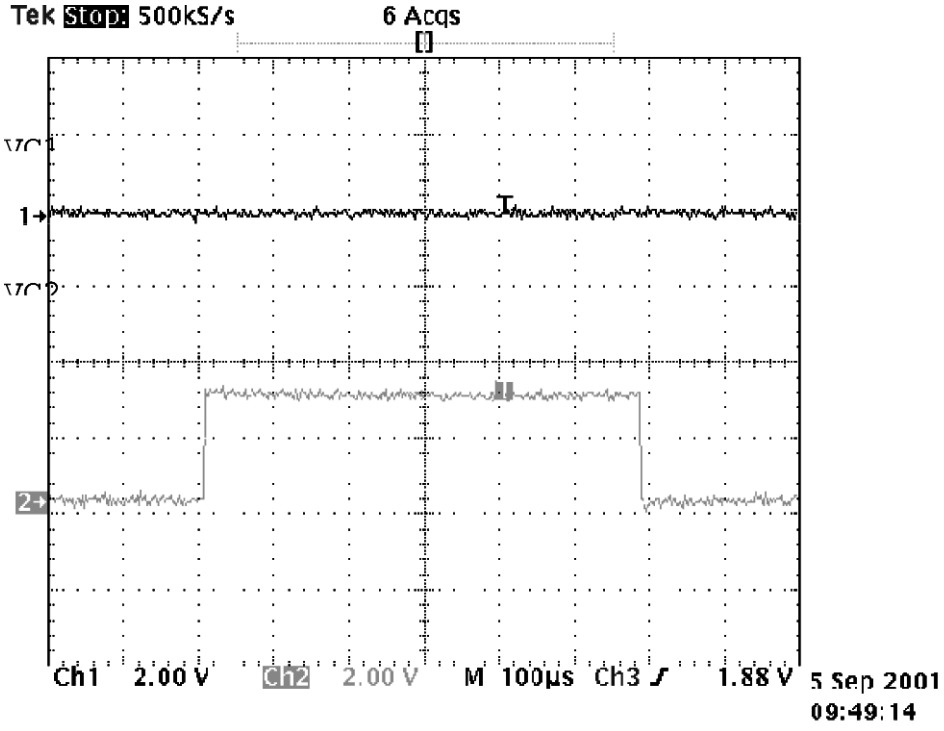


Figure 3-17. Control Signal of FEM in DCS TX mode.

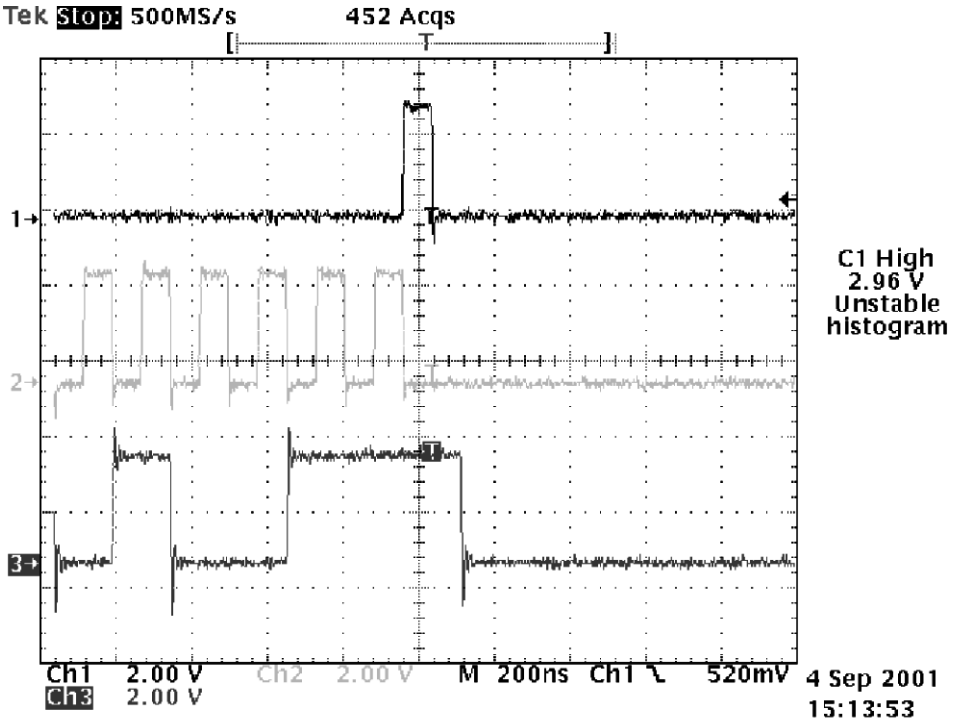


Figure 3-18. LE, Clcok, Data.

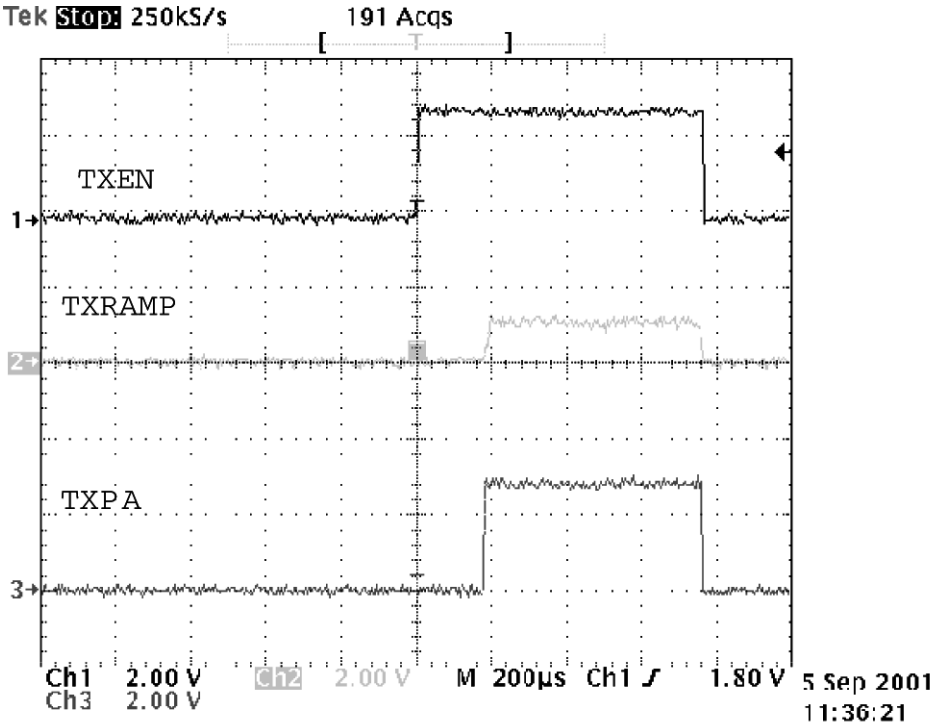


Figure 3-19. TXEN, TARAMP, TXPA.

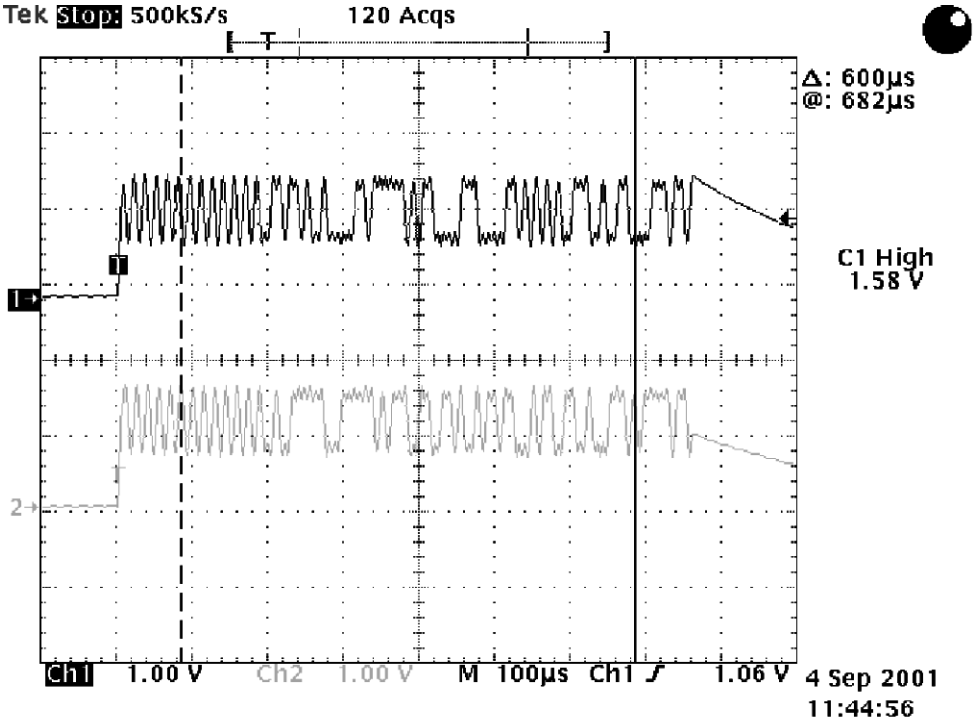
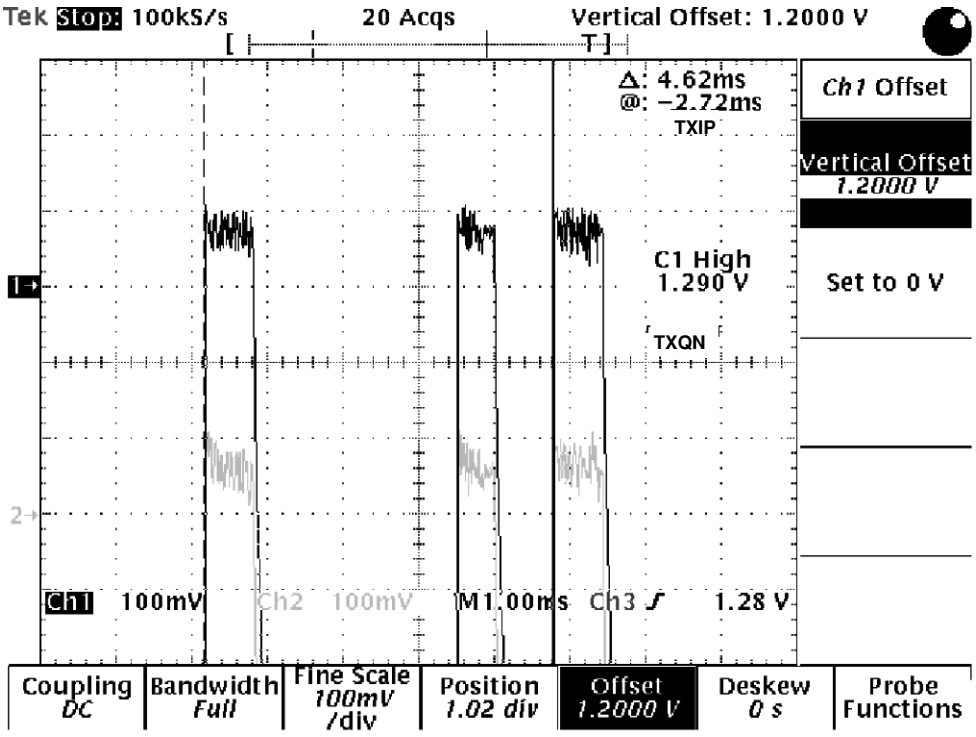


Figure 3-20. TX IQ Signal.



7Figure 3-21. RX IQ Signal.

3.7 Digital Main Processor

The AD6522 is an ADI designed processor.

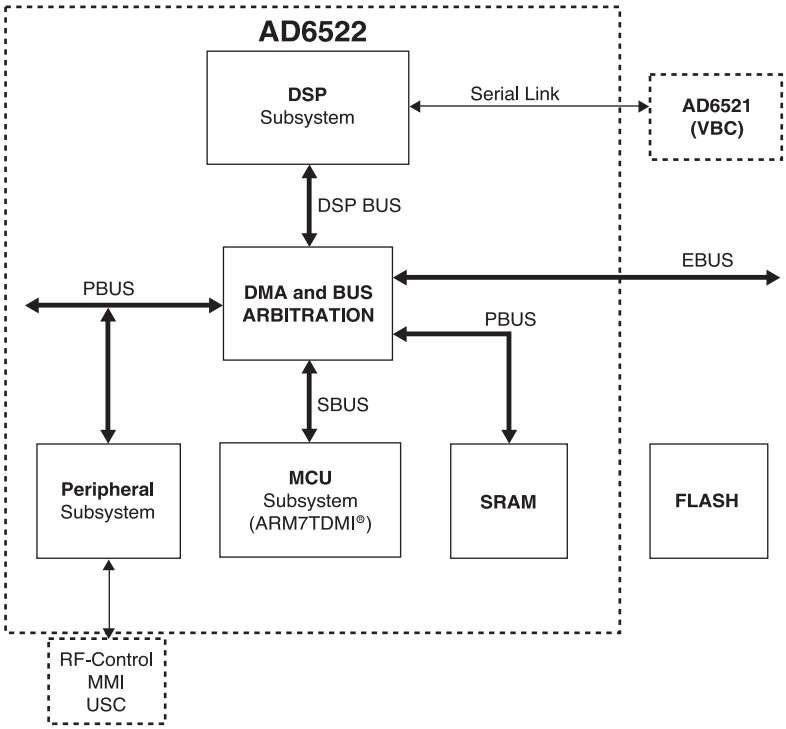


Figure 3-22. Top level block diagram of the AD6522 internal architecture.

BUS Arbitration Subsystem

- It is to work as a cross point for data accesses between the three main busses.
- EBUS is for external accesses, primarily from Flash memory for code and data.
- RBUS is for internal RAM access
- PBUS is for access to internal peripheral modules such as UART, RTC or SIM.
- In addition to the three main system busses, it has SBUS, IOBUS and DMABUS.

DSP subsystem

- It consists of ADI DSP, Viterbi coprocessor, Ciphering unit and a cache memory/controller system
- The DSP can run at a maximum clock frequency of 78MHz at 2.45V
- The Viterbi and ciphering accelerators enable a very efficient implementation of the channel equalization, encryption and decryption tasks.

MCU subsystem

- It consists of an ARM7TDMI central processing unit, a boot ROM, a clock generation and access control module.
- The maximum clock frequency for the ARM7TDMI is 39MHz at 2.45V
- The main clock is 13MHz and it is provided by VCTCXO. The Clock & BS(Bus Select) generator make internal clock by multiplying the main clock by 1X, 1.5X, 2X and 3X
- The boot ROM contains MCU code for basic communication between the ARM and one of the serial ports in the Universal System Connector subsystem.

Peripheral subsystem

- It contains four major groups of elements.
- The MMI group is a collection of all the functionality that are needed to implement a complete user interface including keyboard, display, backlight, RTC, general purpose I/O etc.
- House Keeping group consists of three different sub-modules: The Watch Dog Timer, the Interrupt Controller, and the general timers.
- GSM system group consists of the time base generation together with the synthesizer interface, which form the radio control.
- Direct Memory Access is located between the three system buses(PBUS, RBUS and EBUS) and can move any data from any address location on one system bus to any address location on another system bus.

Interconnection with external devices

RTC block interface

Countered by external X-TAL(32.768KHz)

LCD module interface

	Description
LCD_MAIN_CS	LCD chip enable
LCD_RES	This pin resets LCD module
LCD_RS	This pin determines whether the data to LCD module is display data or control data
_WR,_RD	Read/Write control
DATA[00…07]	Parallel data line

Memory interface.

16 bit parallel interface.

Addressing ADD01 ~ ADD21.

SIM interface

The AD6522 check status periodically in call mode if SIM card is inserted, but the AD6522 don't check in deep sleep mode.W3000 support only 3.0 volt interface SIM card.

Key interface

Include 5 column and 5 row The AD6522 detect key press by interrupt.

AD3408 interface

EOC : End Of Charge. Charging would be stopped when AD6522 receive this signal.

CHARGERDETECT: This interrupt is generated when charger is inserted

RF interface

The AD6522 control RF parts through TXEN, RXEN, AGCEN etc.

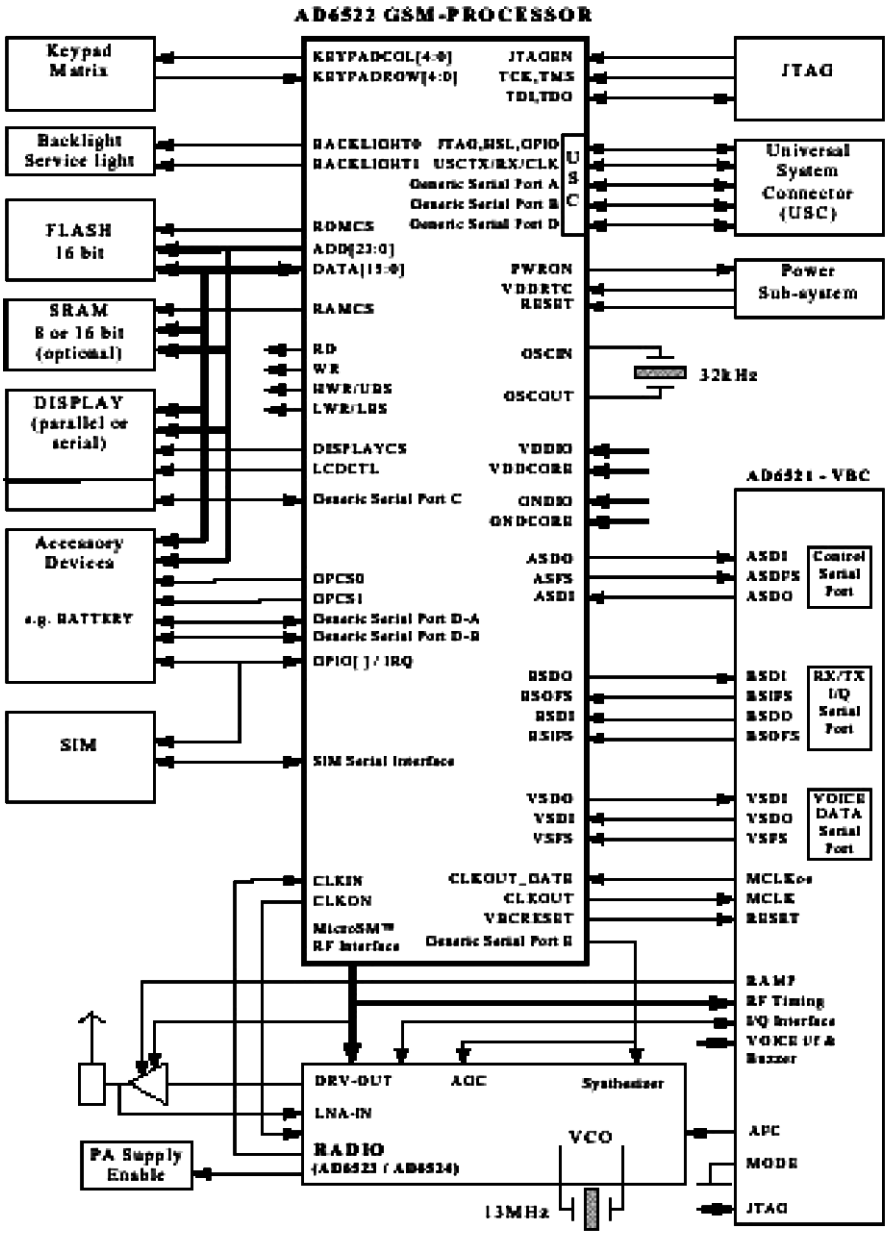


Figure 3-23. System interconnection of AD6522 external interfaces

3.8 Analog Main Processor

Baseband Transmit/ Receive section

This section generates I/Q inputs/outputs modulated GMSK signals in accordance with GSM 05.05 Phase 2 specifications.

- The transmit path consist of a GMSK modulator and two high speed DACs with output reconstruction filters.
- The receive path consists of two resolution sigma-delta ADCs which include high performance digital filters for RF channel selection

Auxiliary section

This section contains two auxiliary DACs(AFC DAC,IDAC) for system control.

- AFC(automatic frequency control) of master clock oscilator
- IDAC : gernerate analog signal for battery charging

AUX ADC : 6 channel 10 bits

AFC DAC : 13 bits

IDAC : 10 bits

Voiceband section

Receive audio signal from MIC, Send audio signal to Receiver.

It interconnect with external device like main microphone(VINNORP, VINNORN), main receiver(VOUTNORP, VOUTNORN), Hands free kit mic(VINAUXP, VINAUXN) and Hands free kit speaker(VOUTAUXP, VOUTAUXN).

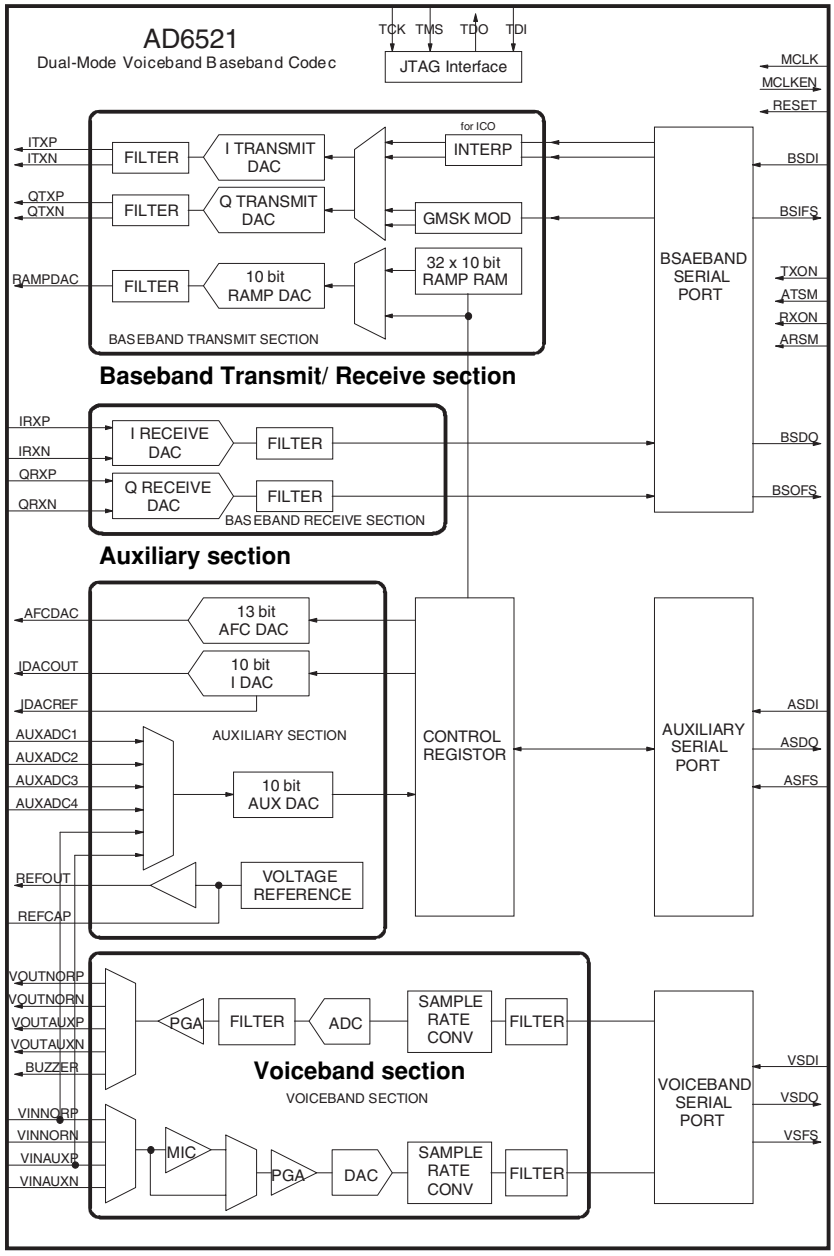

AD6521
Dual-Mode Voiceband Baseband Codec
TCK TMS TDO TDI
JTAG Interface
MCLK
MCLKEN
RESET
for ICO
ITXP
ITXN
FILTER
I TRANSMIT DAC
INTERP
QTXP
QTXN
FILTER
Q TRANSMIT DAC
GMSK MOD
RAMPDAC
FILTER
10 bit RAMP DAC
32 x 10 bit RAMP RAM
BASEBAND TRANSMIT SECTION
BSAEBAND SERIAL PORT
BSDI
BSIFS
TXON
ATSM
RXON
ARSM
Baseband Transmit/ Receive section
IRXP
IRXN
QRXP
QRXN
I RECEIVE DAC
Q RECEIVE DAC
FILTER
FILTER
BASEBAND RECEIVE SECTION
BSDQ
BSOFS
Auxiliary section
AFCDAC
IDACOUT
IDACREF
13 bit AFC DAC
10 bit I DAC
AUXILIARY SECTION
AUXADC1
AUXADC2
AUXADC3
AUXADC4
10 bit AUX DAC
REFOUT
REFCAP
VOLTAGE REFERENCE
CONTROL REGISTOR
AUXILIARY SERIAL PORT
ASDI
ASDQ
ASFS
VOUTNORP
VOUTNORN
VOUTAUXP
VOUTAUXN
BUZZER
PGA
FILTER
ADC
SAMPLE RATE CONV
FILTER
Voiceband section
VOICEBAND SECTION
VINNORP
VINNORN
VINAUXP
VINAUXN
MIC
PGA
DAC
SAMPLE RATE CONV
FILTER
VOICEBAND SERIAL PORT
VSDI
VSDQ
VSFS

Figure 3-24.

3.9 Power management

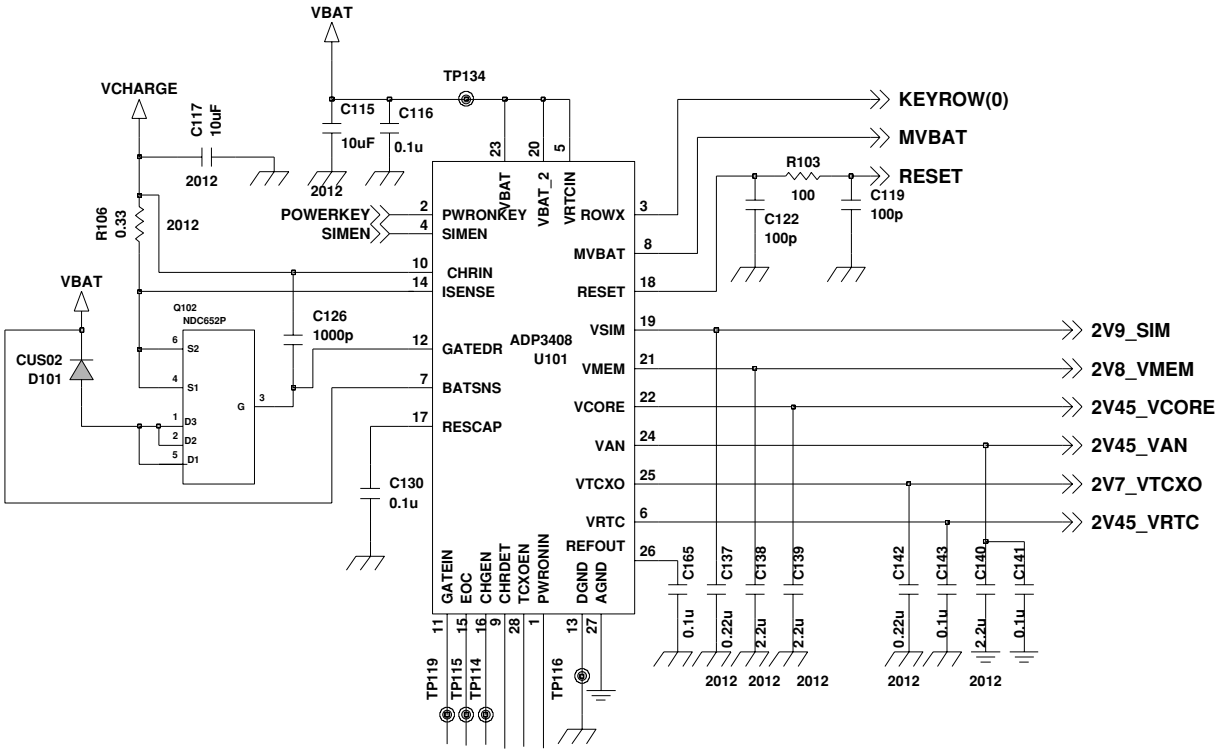


Figure 3-25

LDO block

	Description
VSIM	2.86 V (is provided to SIM card)
VCORE	2.45 V (is provided to the AD6522 & AD6521's digital core)
VRTC	2.45 V (is provided to the RTC and Backup Battery)
VAN	2.45 V (is provided to the AD6521 I/O and used as microphone bias)
VTCXO	2.715 V (is provided to VCTCXO)
VMEM	2.80 V (is provided to Flash)

There are 6 LDOs in the ADP3408

Power up sequence logic

• The ADP3408 controls power on sequence If a battery is inserted, the battery powers the 6 LDOs. Then if PWRONKEY is detected, the LDOs output turn on.
Reset is generated and send to the AD6522

Battery charging block(W3000 use Li-Ion battery only.)

• Charger initialization, trickle charging, and Li-Ion charging control are implemented in hardware.

• Charging Process

1. Check charger is inserted or not

2. If ADP3408 detects that Charger is inserted, AD3408 Detect Signal output is HIGH

3. Start CC charging (HIGHCURRENT CHARGE MODE)

4. if VBAT>4.2V, end of charge, then EOC(AD3408Output) is HIGH

if VBAT < UVLO, then charging in Low Current Charge Mode, until VBAT > UVLO(**Under voltage lock out**)

The Status of charging is displayed in the LCD by connecting MVBAT in AD3408 and AD6521.

• Pins used for charging

CHG_DET : Interrupt to AD6522 when charger is plugged.
CHG_EN : Control signal from AD6522 to charge Li+ battery
EOC : Interrupt to AD6522 when battery is fully charged
GATEIN : Control signal from AD6522 to charge NiMH battery. But, not used.
MVBAT : Battery voltage divider. Divide ratio is 1:2.3 and it is sensed in AD6521 AUX_ADC

• TA (Travel Adaptor)

Input voltage : AC 85V ~ 260V, 50~60Hz
Output voltage : DC 5.2V(°æ0.2 V), Output current: Max 850mA(°æ50mA)

• Battery

Li-ion battery(Max 4.2V, Nom 4.0V, Capacity - 850mAh)

LDO block

There are 6 LDOs in the ADP3408

Battery charging block

It can be used to charge Lithium Ion and/or Nickel Metal Hydride batteries. W3000 use Li-Ion battery only. Charger initialization, trickle charging, and Li-Ion charging control are implemented in hardware.

Charging Process

Check charger is inserted or not. If ADP3408 detects that Charger is inserted, the CC-CV charging starts.

Exception: When battery voltage is lower than 3.2V, the precharge (low current charge mode) starts firstly. And the battery voltage reach to 3.2V the CC-CV charging starts.

Pins used for charging

CHRDET: Interrupt to AD6522 when charger is plugged.

CHGEN: Control signal from AD6522 to charge Li+ battery

EOC: Interrupt to AD6522 when battery is fully charged

GATEIN: Control signal from AD6522 to charge NiMH battery. But, not used.

MVBAT: Battery voltage divider. Divide ratio is 1:2.3 and it is sensed in AD6521 AUX_ADC4

TA (Travel Adaptor)

Input voltage: AC 85V ~ 260V, 50 ~ 60Hz

Output voltage: DC 5.2V (±0.2 V)

Output current: Max 850mA (±50mA)

Battery

Li-ion battery (Max 4.2V, Nom 4.0V)

Standard battery : Capacity - 850mAh, Li-ion

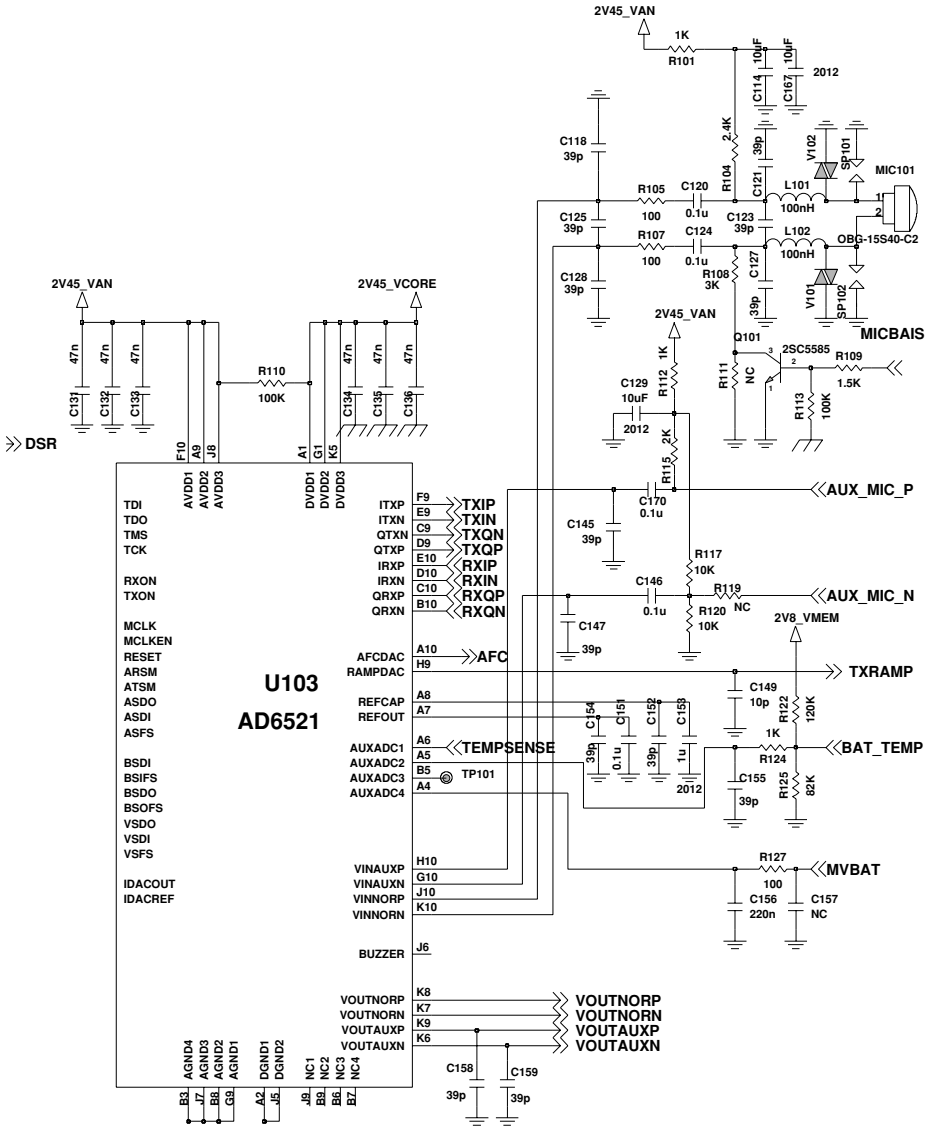


Figure 3-26. AD6521 Circuit diagram

3.10 Memories

32M flash memory + 8M SRAM

16 bit parallel data bus

ADD01 ~ ADD21.

RF Calibration data are stored in Flash

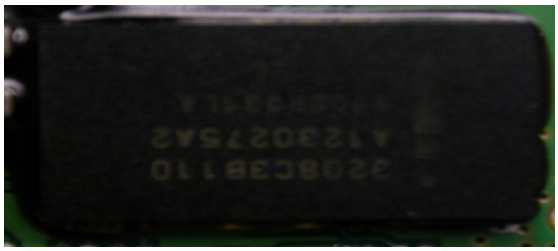


Figure 3-27

3.11 Display and Interface

- W3000 has one LCD.
- There are the control output LCD_MAIN_CS which is derived from AD6522, this acts as the chip select enable for the LCD.
- AD6522 uses DATA[00:07] pins to send data for displaying graphical text onto the LCD.
  : LCD : 128 x 64 dots + 1 hard icon
  BLUE color LED backlight X 2 X 2

3.12 Keypad Switches and Scanning

The key switches are metal domes, which make contact between two concentric pads on the keypad layer of the PCB when pressed. There are 19 switches, connected in a matrix of 5 rows by 5 columns, as shown in Figure, except for the power s witch (KB310), which is connected independently. Functions, the row and column lines of the keypad are connected to ports of AD6522. The columns are outputs, while the rows are inputs and have pull-up resistors built in. When a key is pressed, the correspon ding row and column are connected together, causing the row input to go low and generate an interrupt. The columns/ rows are then scanned by AD6522 to identify the pressed key.

KEY PAD

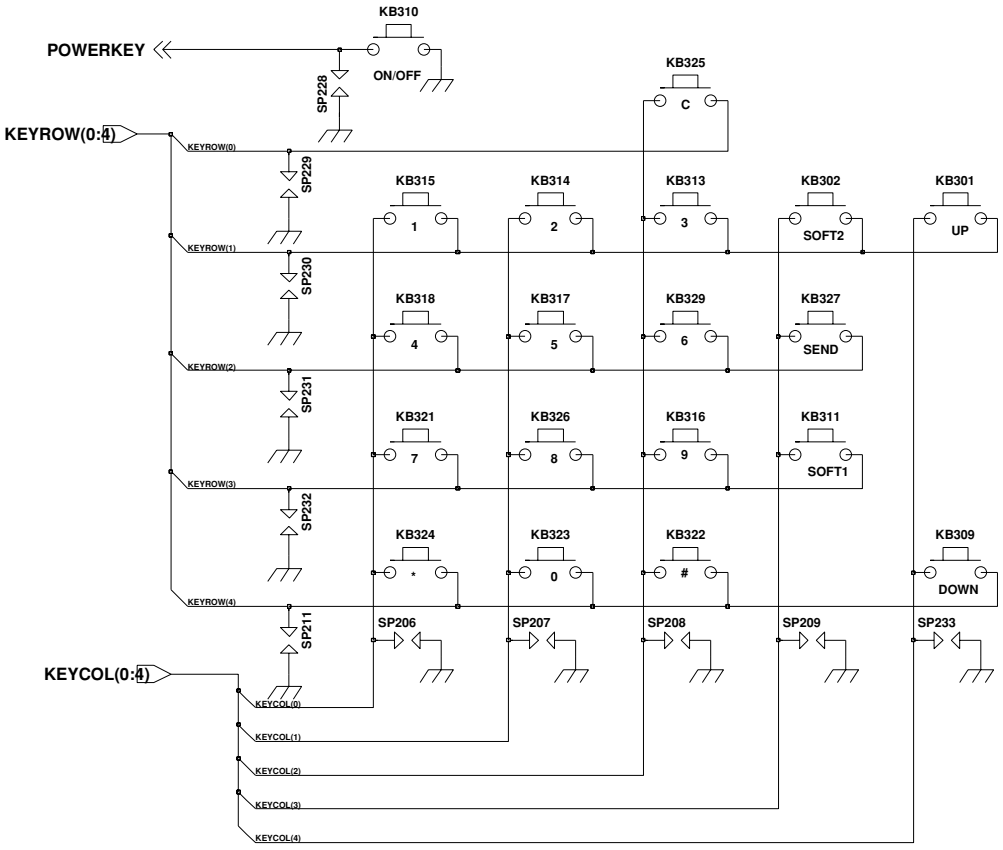


Figure 3-28

3.13 Microphone

The audio signal is passed to VINNORP and VINNORN pins of AD6522.

The voltage supply 2V45_VAN is output from ADP3408, and is a bias voltage for both the VINNOR (through R101) and VINAUX (through R112) lines.

The VINNOR or VINAUX signal is then A/D converted by the Voiceband ADC part of AD6521.

The digitized speech is then passed to the DSP section of AD6522 for processing (coding, interleaving etc.).

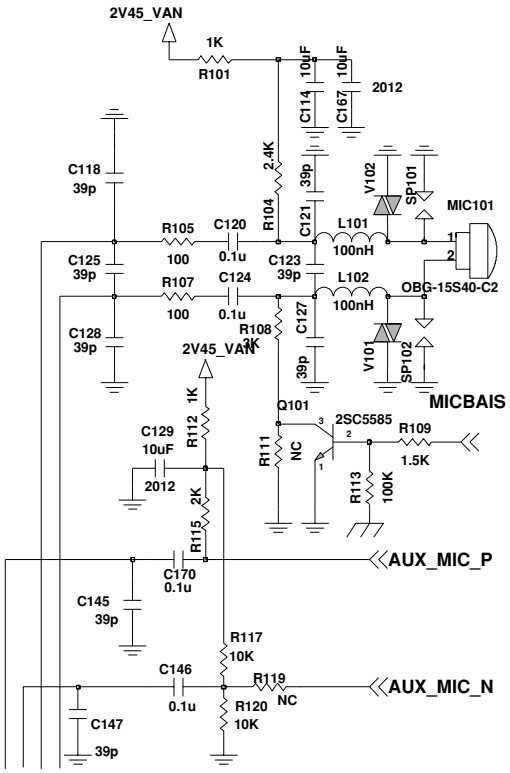


Figure 3-29

3.14 Earpiece & Handsfree

The earpiece is driven directly from AD6521 VOUTNORP and VOUTNORN pins and the gain is controlled by the PGA (Programmable Gain Amplifier) in an AD6521.

The audio out (VOUTAUXP & VOUTAUXN) to the hands-free kit consists of a pair of differential signals from AD6521 auxiliary outputs, which are tracked down the board to carkit connector(CN302) at the base of the handset.

The DC level of the signal is supplied to the VOUTAUX pin.

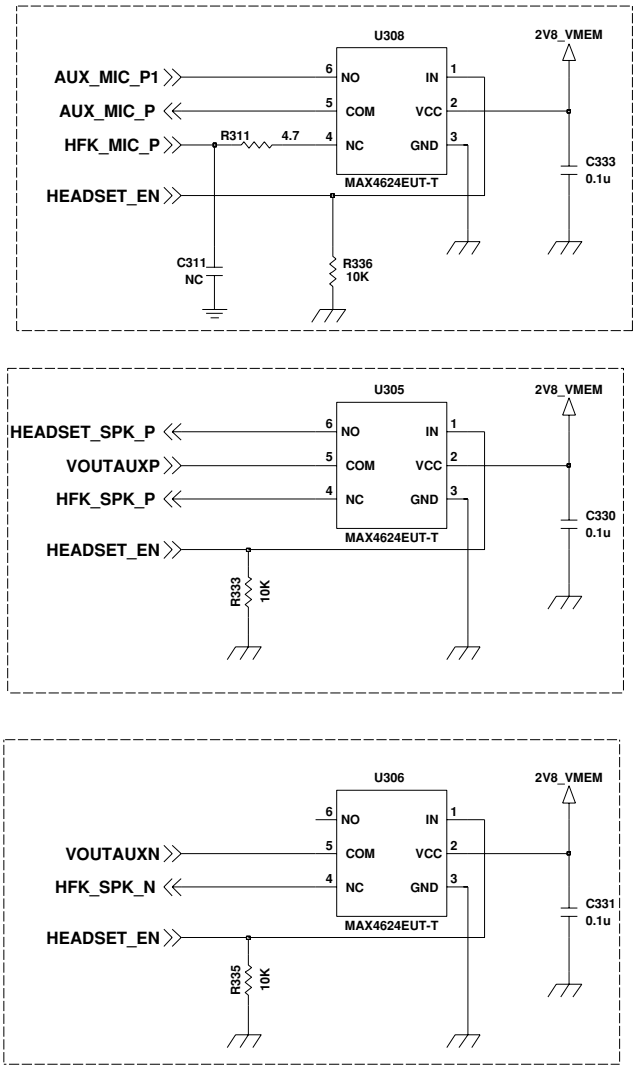
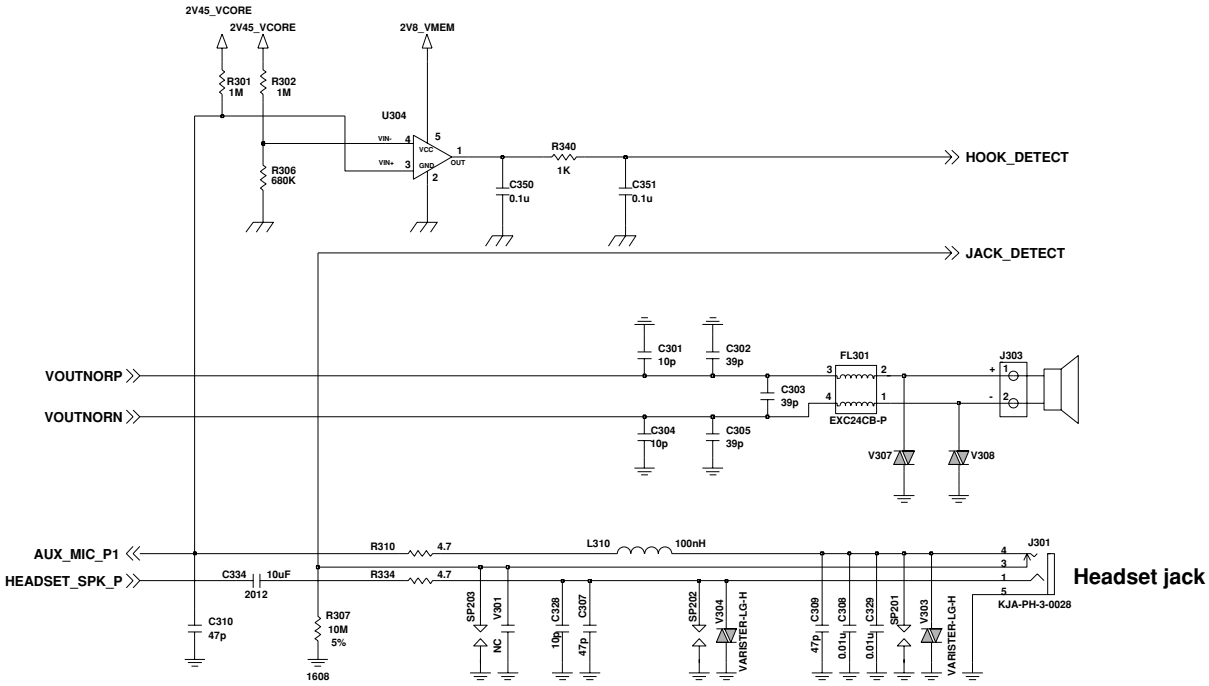


Figure 3-30



MAX4624 ACTIVE

IN	NC(4)	NC(6)
H	OFF	ON
L	ON	OFF

Figure 3-31

3.16 Headset Jack Interface

3.17 Key Back-light Illumination

In key back-light illumination, there are 6 White LEDs in Board, which are driven by KEY_BACKLIGHT line from AD6522.

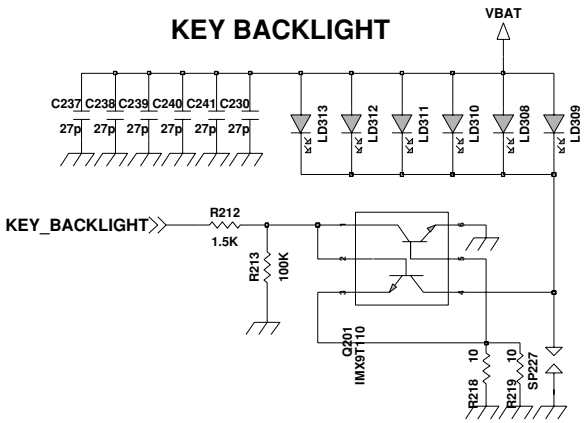


Figure 3-32. Key Back-light Illumination.

3.18 LCD Back-light Illumination

In LCD Back-light illumination, there is an driver in FPCB Board, which is driven by BACKLIGHT line from AD6522.

3.19 Speaker & MIDI IC

W3000 don't use buzzer. Instead use loud speaker and Melody IC which support handsfree function and various melody sound.

• Melody IC control

5 GPIO is assigned to control melody IC. Melody data is transferred to melody IC and played by loud phone.

• External 3.3V LDO

The maximum output current of analog amplifier in melody IC is 300mA.

The current can not be fed by internal Omega so external LDO(U303) is included for max power of loud Speker.

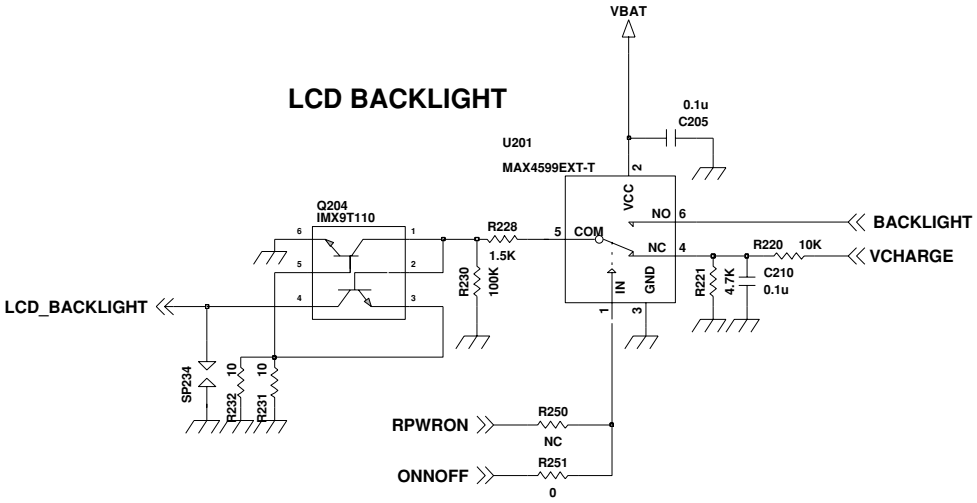


Figure 3-33. Speaker & MIDI IC

MA-3 is a synthesizer LSI for mobile phones that realize advanced game sounds. This LSI has a built-in speaker amplifier, and thus, is an ideal device for outputting sounds that are used by mobile phones in addition to game sounds and ringing melodies that are replayed by a synthesizer. The synthesizer section adopts “stereophonic hybrid synthesizer system” that are given advantages of both FM synthesizers and Waveform table synthesizers to allow simultaneous generation of up to thirty-two FM tones and eight Waveform table tones. Since FM synthesizer is able to present countless tones by specifying parameters with only several tens of bytes, memory capacity and communication band can be saved, and thus, the device exhibits the features in operating environment of mobile phones such as allowing distribution of arbitrary melodies with tones. On the other hand , since Waveform table synthesizer complies with downloading of tones from host CPU, arbitrary ADCM/PCM tones can be treated from sequencer in addition to the use of tones that are built-in the LSI.

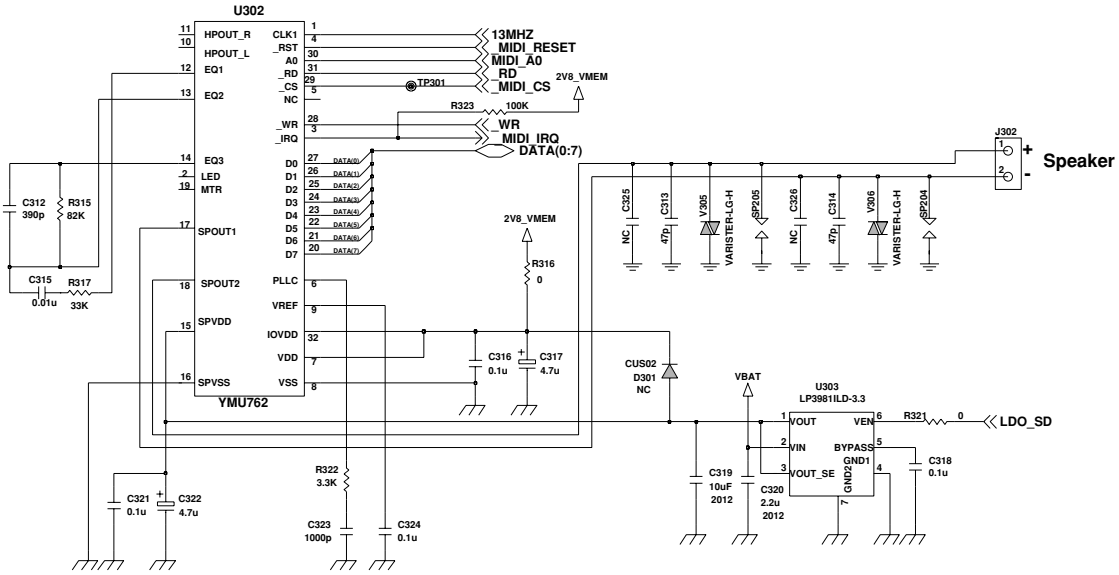


Figure 3-34