SL55

Level 2.5e

Repair Documentation

V 1.0

Version	Date	Department	Notes to change
V 1.00	June 2003	ICM MP CCQ GRM	New document

Table of Contents:

1 List of available level 2,5e parts SL55

ID-No	Type	Name, Location	Part-No.
D171	IC	EGOLD+ V3.1 F M42	V39197-F5019-F415
V151	Diode	Diode_KB7	V20840-D5062-D670
Z172	Quarz	Quarz EGOLD+	V30145-F102-Y10
R212	Varistor	Varistor IO connector	V39197-F5015-F351
R213	Varistor	Varistor IO connector	V39197-F5015-F351
R215	Varistor	Varistor IO connector	V39197-F5015-F351
R140	Resistor	Resistor Sound/Clock	V24852-C -X
R160	Resistor	Resistor PaRamp	V24852-C -X
R172	Resistor	Resistor Quarz EGOLD+	V24852-C -X
R216	Resistor	Resistor Audio	V24852-C -X
R217	Resistor	Resistor Audio	V24852-C -X
R630	Resistor	Resistor PA	V24852-C -X
R659	Resistor	Resistor RX	V24852-C -X
R662	Resistor	Resistor RX	V24852-C -X
R707	Resistor	Resistor AFC	V24852-C -X
R728	Resistor	Resistor VREGRF2	V24852-C -X
Z211	Filter	Logic/IO_Interface	V39197-F5000-F116
D400	IC	Application_Processor	V20820-L6117-D670
V190	Diode	Diode_SIM Interface	V20840-D53-D670
V191	Diode	Diode_SIM Interface	V20840-D53-D670
V320	Diode	Diode_Akku/Vibra	V20840-D53-D670
N281	IC	Volt.Regulator_Light	V20810-C6106-D670
N282	IC	Volt.Regulator_Light	V20810-C6098-D670
V212	Transistor	Transistor _Light	V20830-C1112-D670
V213	Transistor	Transistor _Vibra	V20830-C1112-D670
V361	Transistor	Transistor_Charger	V20830-C1110-D670
N361	IC	Vol.Regulator	V20810-C6105-D670
D361	IC	ASIC_Salzburg light	V30145-J4682-Y47
R192	Resistor	Resistor_ SIM Interface	V24842-C -X
R376	Resistor	Resistor_ASIC	V24842-C -X
R608	Resistor	Resistor_PA switch	V24842-C -X
R730	Resistor	Resistor VREGRF1	V24842-C -X
Z600	IC	Power_Amplifier	V39197-F5005-F487
D650	IC	Ant_Switch_Diplexer	V39197-F5006-F936
R700	Resistor	Temp_Resistor	V39120-F4223-H
Z700	Quartz	Oszillator_26MHz	V39197-F5007-F381
V700	Diode	Capa_Diode	V20840-D68-D670
D720	IC	Tranceiver	V39197-F5014-F603
Z680	Filter	RX Filter	V39197-F5005-F917

D750	VCO	TX VCO	V20820-L6109-D670
Z750	Filter	TX Filter	V30145-K280-Y242
S851	Switch	Magnetic switch RF	V39197-F5008-F63
S852	Switch	Magnetic switch Logic	V39197-F5008-F63

2 Required Equipment for Level 2,5e

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A1)
- Troubleshooting Frame SL55 (F30032-P260-A1)
- Power Supply
- Spectrum Analyser min. 4GHz
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

Reference: Equipment recommendation V1.2
(downloadable from the technical support page)

3 Required Software for Level 2,5e SL55

- Windows NT Version4
- Winsui version1.42 or higher
- Software for GSM-Tester (Cats(Acterna/Wiltek) or CMU-GO(Rohde&Schwarz))
- Software for reference oscillator adjustment
- Internet unblocking solution
- Dongle driver for USB-Dongle if used with WIN NT4

Information: All software is downloadable from the technical support page

4 Radio Part

The radio part is designed for Tripple Band operation, covering EGSM900, GSM1800 as well as GSM 1900 frequencies, and can be divided into 4 Blocks.

- RF power amplifier (RF9340) and PA Buffer/Limiter (Infineon PMB2256)
- Frontend Module (Epcos M002)
- 26 MHZ reference VCO
- Tranceiver (Infineon Smarti DC PMB 6259 for 900/1800/1900)

  The functionality of the DC SMARTI are:
  - All VCOs and PLLs are build in
  - Direct Modulator
  - Direct Demodulator
  - Including the active part of the reference oscillator.

The RF-Part has it´s own power supply realised by a voltage regulator which is located inside the ASIC. The voltages for the logic part are generated by the Power-Supply ASIC too.

The transmitter part converts the I/Q base band signals supplied by the logic (EGOLD+) into RF-signals with characteristics as defined in the GSM recommendation (www.etsi.org). After amplification by a power amplifier the signal is radiated via the internal antenna.

The receiver part converts the received GMSK signal supplied by the antenna into IQ base band signals which are further processed by the logic (EGOLD+).

The synthesizer generates the required frequencies for the transmitter and receiver. A 26MHz oscillator is acting as a reference frequency.

Restrictions:
The mobile phone can never transmit and receive in both bands simultaneously. Only the monitor time slot can be selected independently of the frequency band. Transmitter and receiver can of course never operated simultaneously.

4.1 Power Supply RF-Part

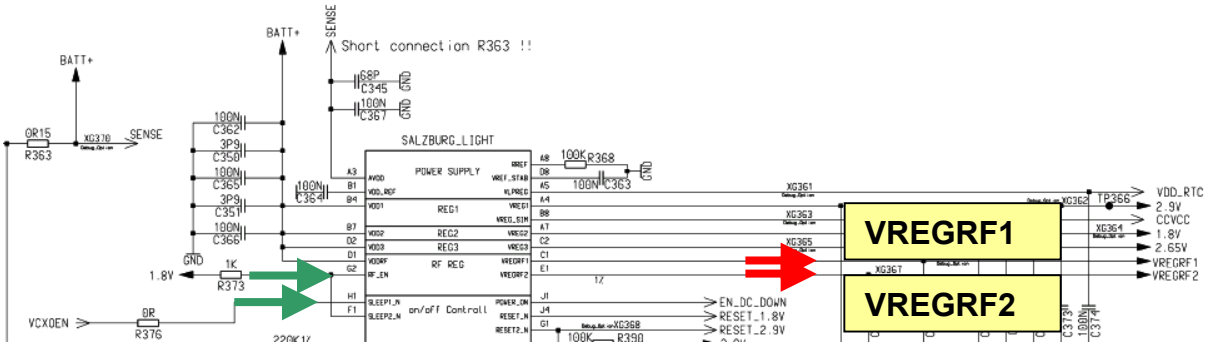
The voltage regulator for the RF-part is located inside the ASIC D361.(see chapter 5.2).It generates the required 2,85V “RF-Voltages” named VREGRF1 and VREGRF2.
The following components are supplied by:

VREGRF1
- 26 MHz reference oscillator
- VCO
- PLL

VREGRF2
- Modulators
- RX mixers
- Limiter amplifier

The voltage regulator RFREG 1 is controlled by 1.8V (RF_EN (RF REG G2)), RFREG2 is controlled by SLEEP1_N (on/off Control H1) and SLEEP2_N (on/off Control F1). IF one of these signals is high the regulator is enable. SLEEP1_N is connected to the signal VCXOEN (Miscellaneous R6) provided by the EGOLD+. RF_EN and SLEEP2_N is connected to 1.8 V provided by the ASIC (REG2 A7) The temporary deactivation is used to extend the stand by time.

Circuit diagram



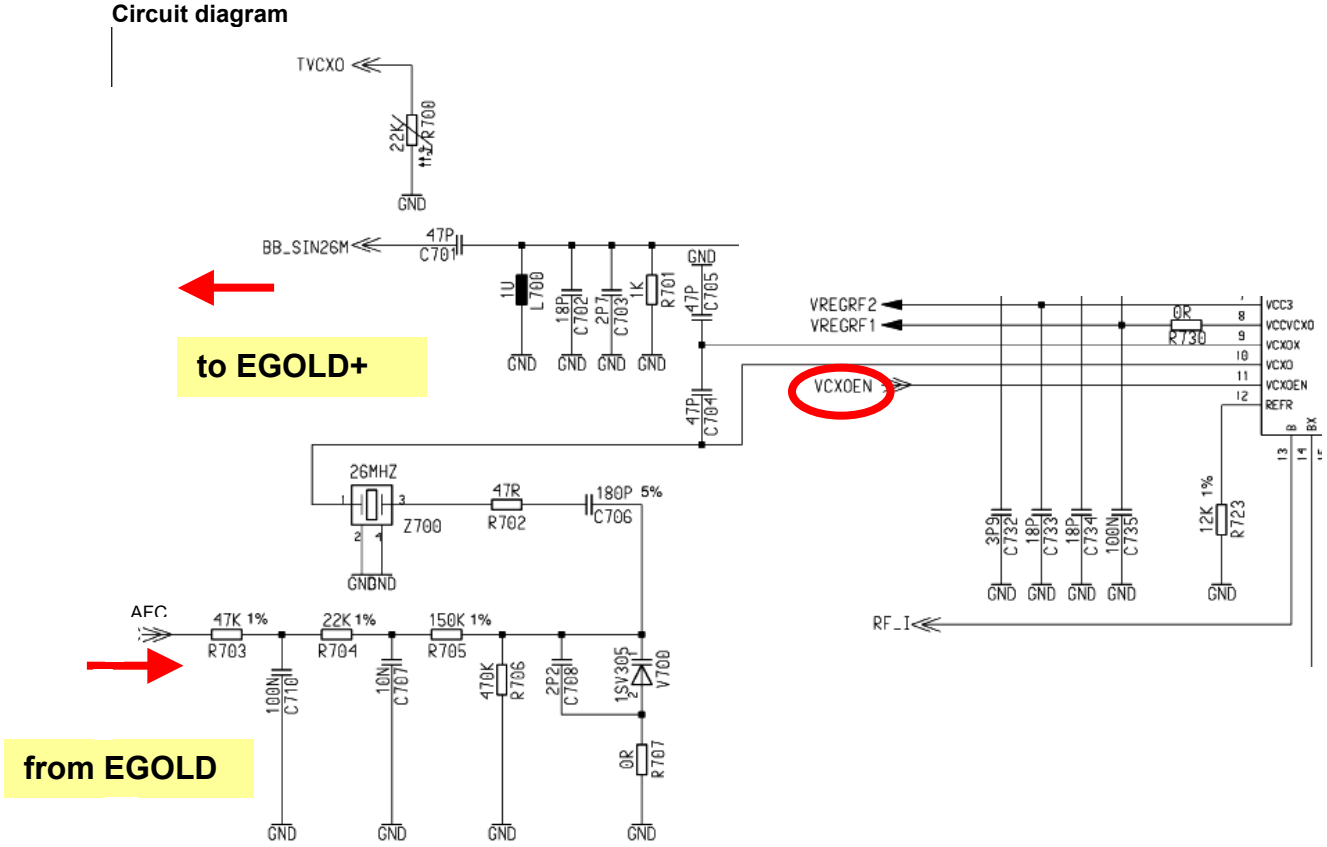
4.2 Frequency generation

4.2.1 Synthesizer: The discrete VCXO (26MHz)

The SL55 mobile phone is using a reference frequency of 26 MHz signal that is created by a partly integrated VCXO. ON/OFF signal (VCXOEN (Miscellaneous R6)) comes from the EGOLD+. A Colpitts-oscillator is used with a post connected buffer stage integrated in the Smarti. For temperature measurements of the VCXO a temperature resistance (R700) is used. The resistor is placed near the VCXO. The measurement result TVCXO is reported to the EGOLD+ (Analog Interface P3) via R138 as the signal TENV.
The frequency of the reference oscillator can be adjusted by the EGOLD+ via a PNM-modulated AFC-signal.
The signal leaves the SMARTI as BB_SIN26M at pin 4 to be further used from the EGOLD+ (D171 (**functional T3**)).

The required voltage VREGRF1 is provided by the ASCI D361

Circuit diagram

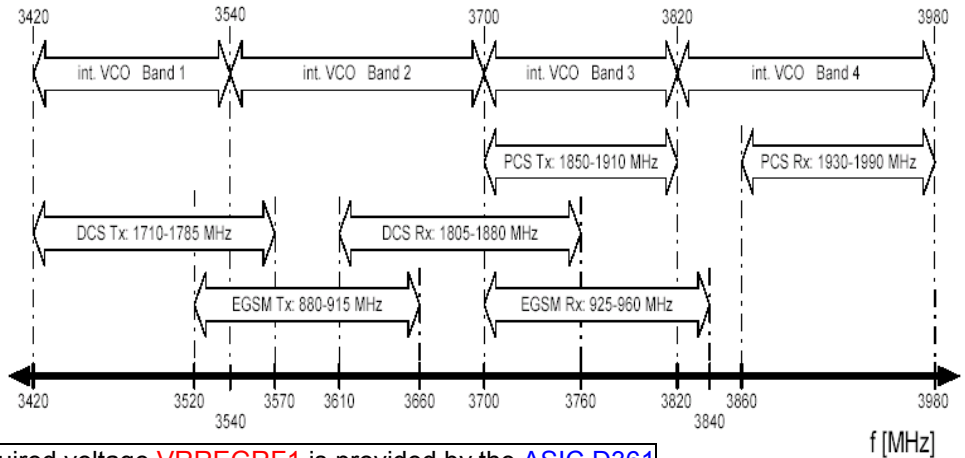


2.2 Synthesizer: LO1

The local oscillator (LO1) consists of a PLL inside the Smarti DC (D720), an external loop filter. The VCO is build in.

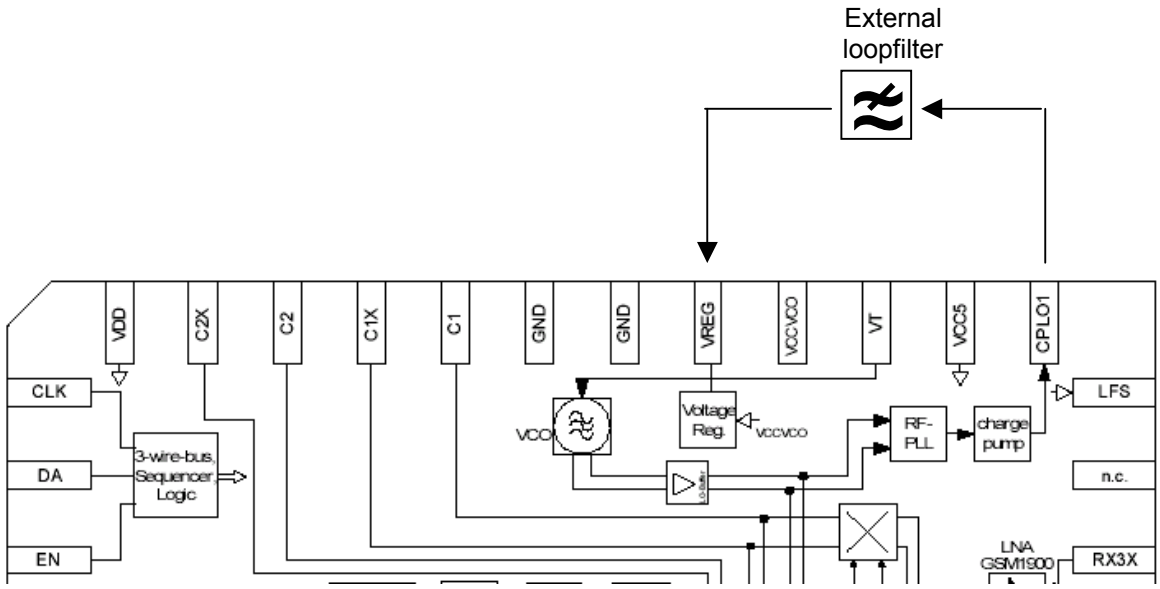
The first local oscillator is needed to generate frequencies which enables the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The LO1/PLL part is switched on with PLLON (**pin 5**) from the EGOLD+ (D171 (**GSM TDMA Timer F16**)). The PLL settings are programmed by the 3 wire bus RFCLK (**pin 1**), RFDATA (**pin2**) and RFSTR (**pin3**). The LO frequency is 4 times the RX/TX frequency for EGSM 900 and 2 times for GSM1800/1900.

This LO1 frequency range

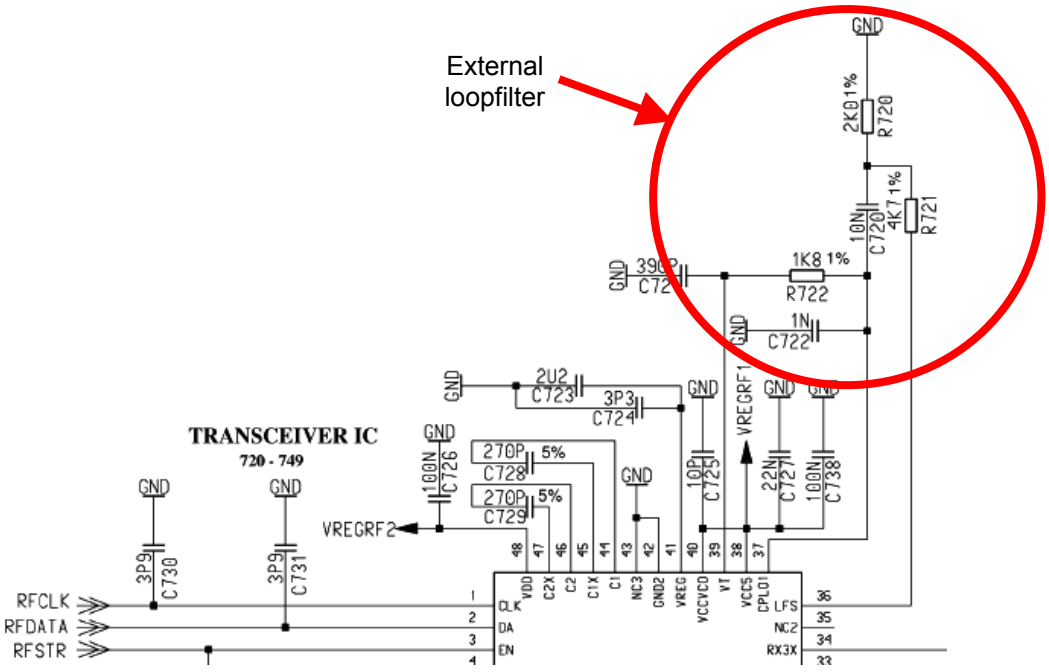


The required voltage VRREGRF1 is provided by the ASIC D361

Block diagram



Circuit diagram



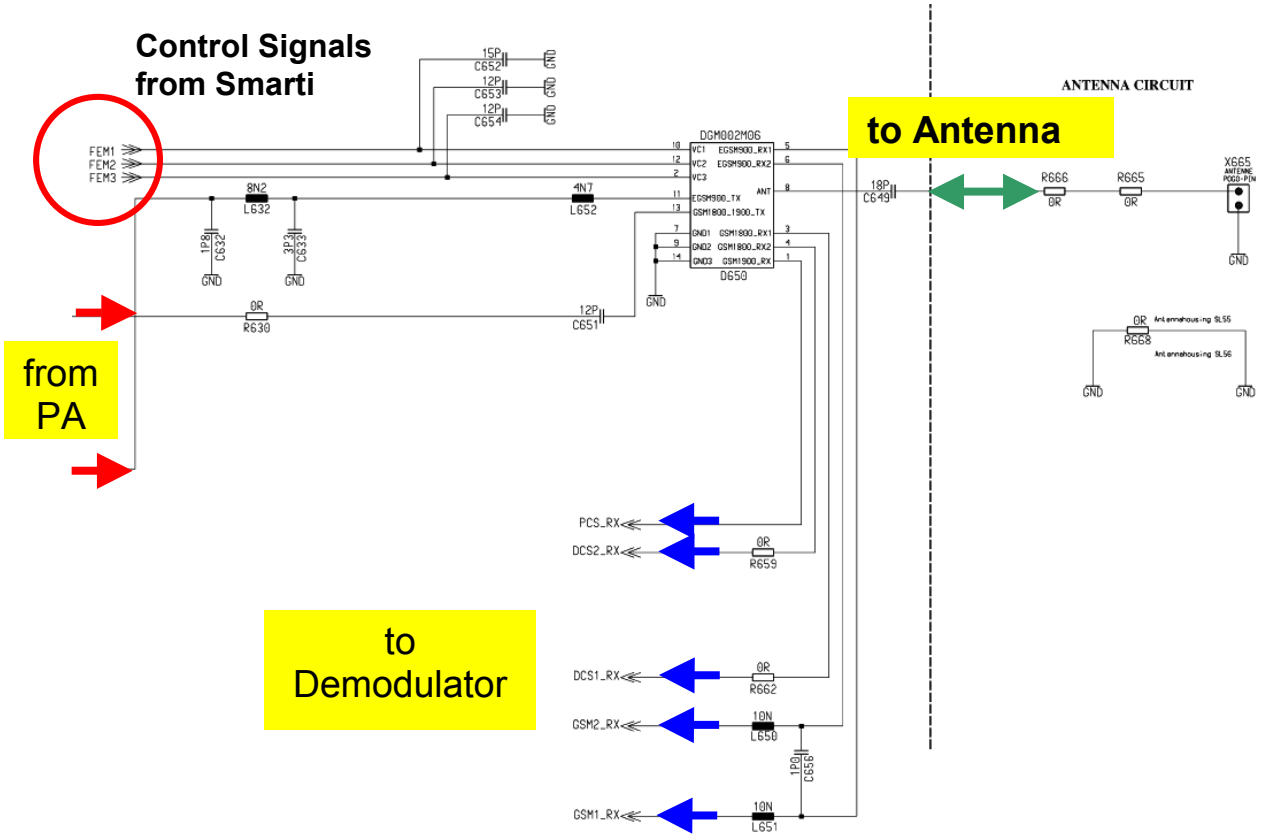
4.3 Frontendmodul (Electrical Antenna Switch)

EGSM900/GSM1800/GSM1900 <> Receiver/Transmitter

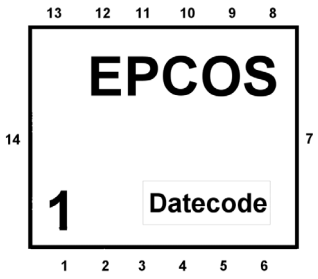
The frontend has two functions.

- to select the different GSM bands
- to switch between RX and TX mode

Inside the frontendmodul SAW filters are integrated in the RX paths.



Mode Selection	FEM 1 / VC1	FEM 2 / VC2	FEM 3 / VC3
EGSM900 RX	LOW	LOW	LOW
EGSM900 RX	HIGH	LOW	LOW
GSM1800 RX	LOW	LOW	LOW
GSM1800 TX	LOW	HIGH	LOW
GSM1900 RX	LOW	LOW	HIGH
GSM1900 TX	LOW	HIGH	LOW

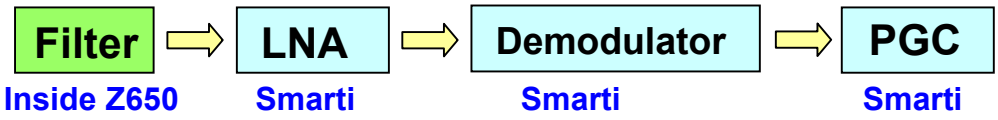


D650
Top View

4.4 Receiver

4.4.1 Receiver: EGSM900/GSM1800/GSM1900 –Filter to Demodulator

From the antenna switch, up to the demodulator the received signal passes the following blocks to get the demodulated baseband signals for the EGOLD+:



Filter: The EGSM900, GSM1800 and GSM 1900 filters are located inside the frontend module. The Filter are centred to a frequency of 942,5MHz for EGSM900, 1847,5MHz for GSM1800 and 1960MHZ for GSM1900.

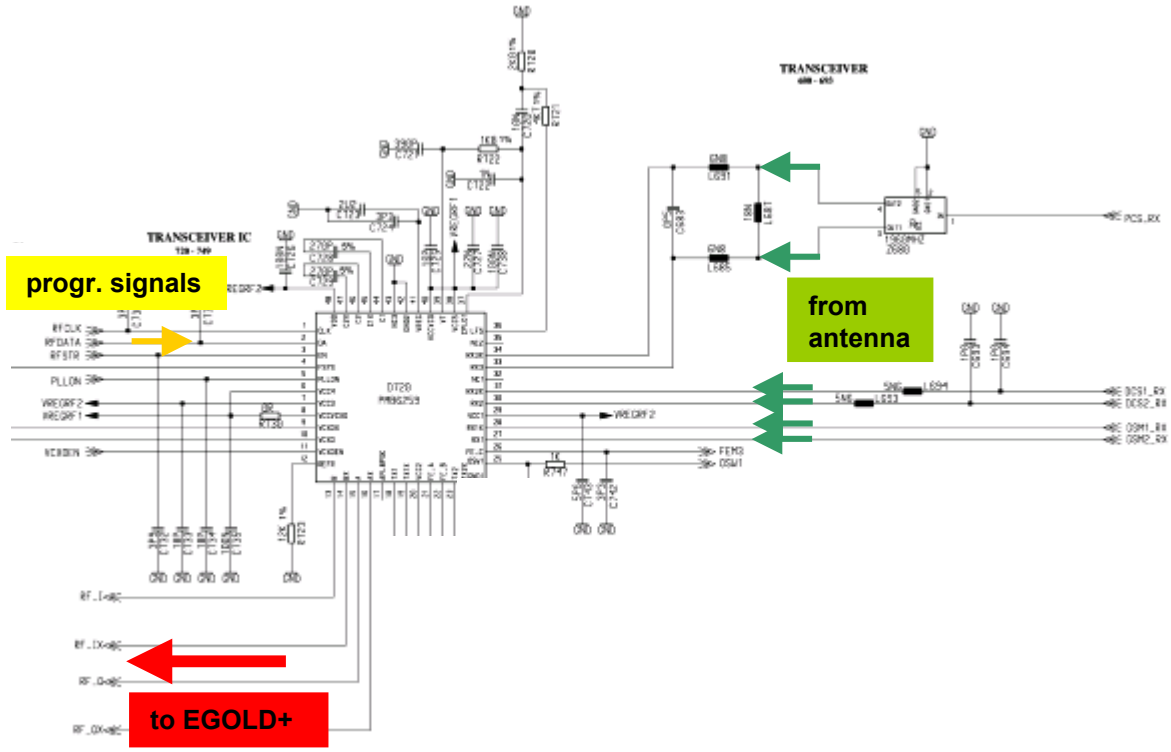
LNA: The LNA´s (EGSM900/GSM1800/GSM1900) are located inside the Smarti. The LNA can be switched in HIGH (On) and LOW (Off) mode and is controlled by the Smarti depending on EGOLD+ information.

Demodulator: The Smarti DC consists of a direct conversion receiver for GSM 900/1800/1900. The amplified RF signal is converted by a quadrature demodulator to the final outputsignals at baseband frequency. The LO signals are generated by a divider by 4 for the GSM900 band and by a divider by 2 for GSM1800 and GSM1900 band.
The resulting in-phase and quadratursignals are fed into two baseband low pass filters and the PGC amplifier chain. The baseband filter provide a suppression of inband-blocking and adjacent channel interferers.

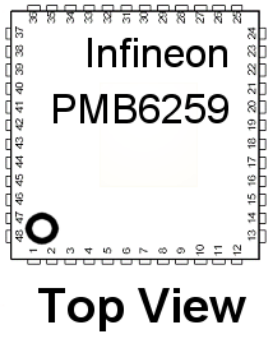
PGC: After baseband filtering the signal is fed into a PGC amplifier chain. The baseband amplifier offers 78 dB programmable gain with 2 dB steps. Due to the high baseband gain (58 dB), DC offsets can corrupt the signal at the baseband outputs. Differential offset voltages are reduced by an internal offset compensation circuit. The control is realised through the EGOLD+ signals (RFDATA; RFCLK; RFSTR.(RF Control J15, J16, J17).

The required voltages VREGRF1 and VREGRF2 are provided by the ASIC D361

Circuit diagram



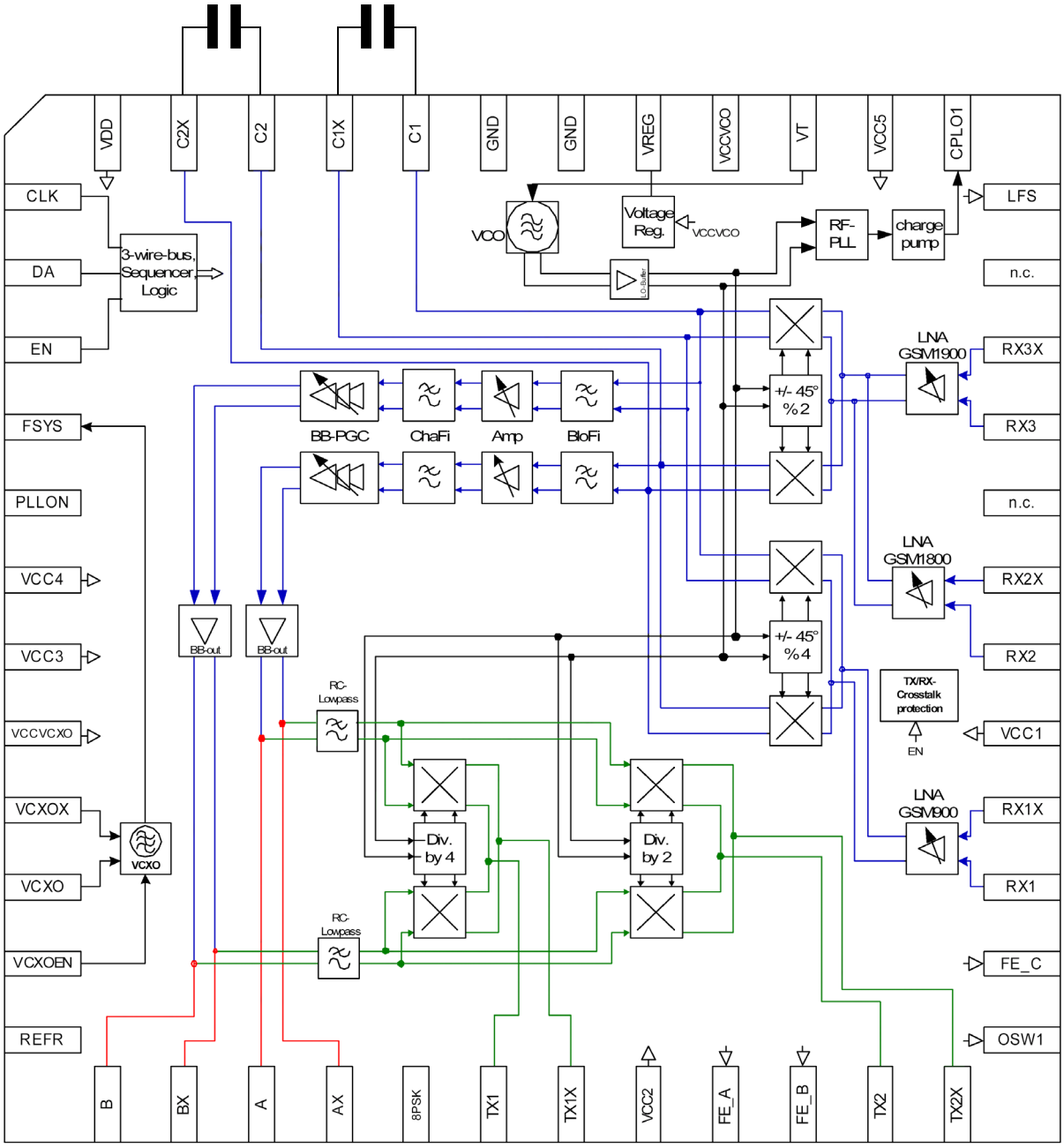
Top view



4.4.2 IC Overview

IC Overview

Smarti



RX Path

TX Path

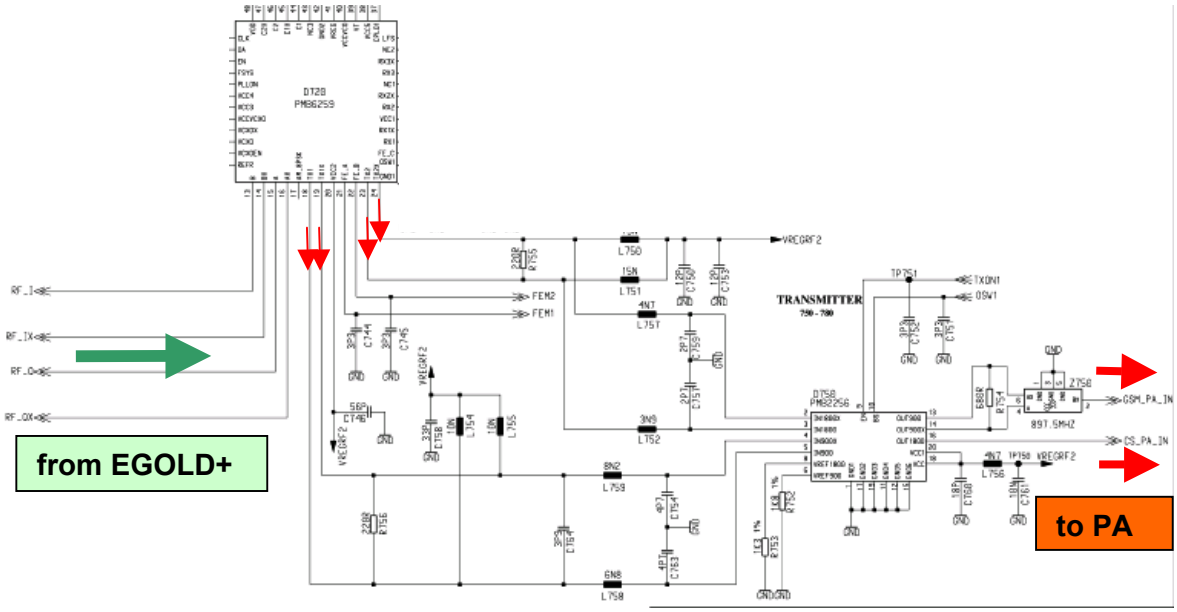
RX/TX Path

4.5 Transmitter

4.5.1 Transmitter: Modulator and Limited Amplifier

The GMSK modulated signal is generated in the direct modulator. That means, that the modulators are working directly on the final output frequency. The LO frequency is divided by 2 or 4, depending on the GSM band. There are two modulators, one for the two higher bands and the other for the two lower bands..

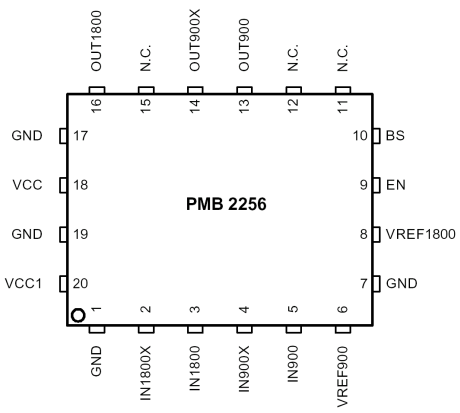
The required voltages VREGRF1 and VREGRF2 are provided by the ASIC D361



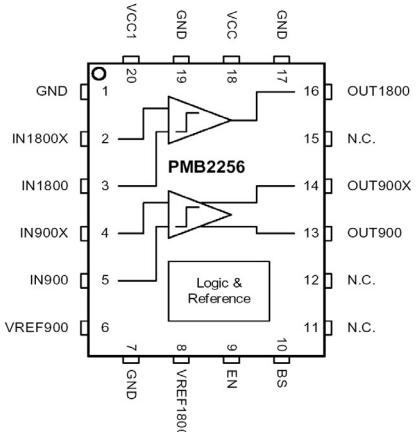
The actual signal is fed into a limiting amplifier with 3 dB amplification which also provides a signal path for the high band and one for the low band.

Mode Selection	Pin9 / EN (TXON1/D171_J14))	Pin10 / BS (OSW1/D720_25)
EGSM900 limiter enable	HIGH	LOW
GSM1800 limiter enable	HIGH	HIGH

Top View



IC Overview



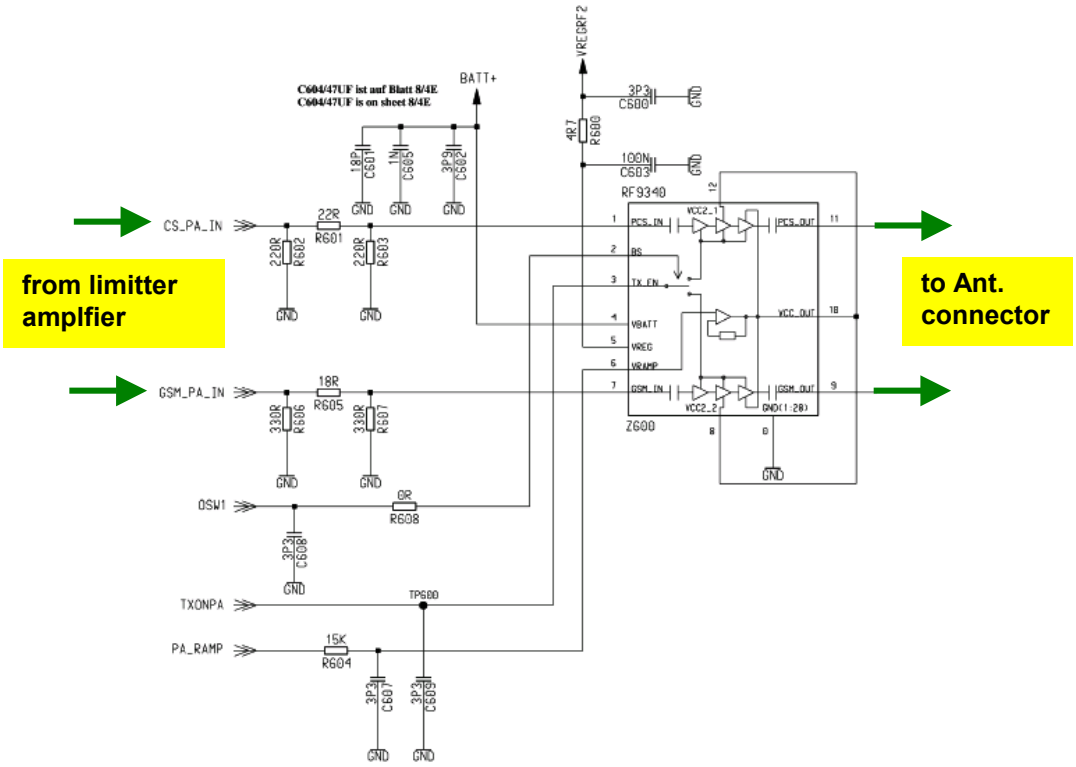
The next stage in the low band line-up is a TX saw filter.

In the high band no SAW filter is required.

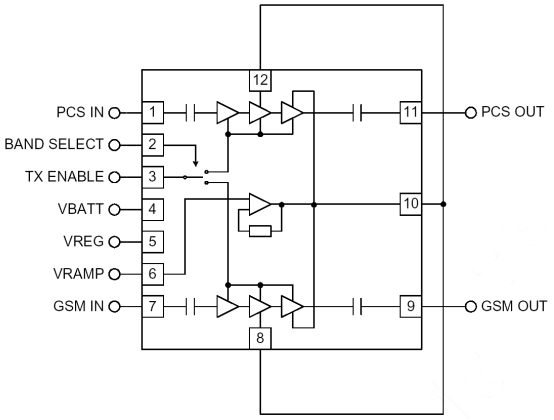
4.5.2 Transmitter: and Power Amplifier

The output signals (CS_PA_IN , and GSM_PA_IN) from the limited amplifier are led to the power amplifier (Z600) passing a matching circuit. contains two separate 3-stage amplifier chains for GSM 850/900 and GSM 1800/1900. The control of the output power is handled via one Vapc port. The power control circuit itself is integrated in the PA module. The EGOLD generates the power control signal PA-RAMP. The band selection switching is done via OSW1 from the Smarti IC.

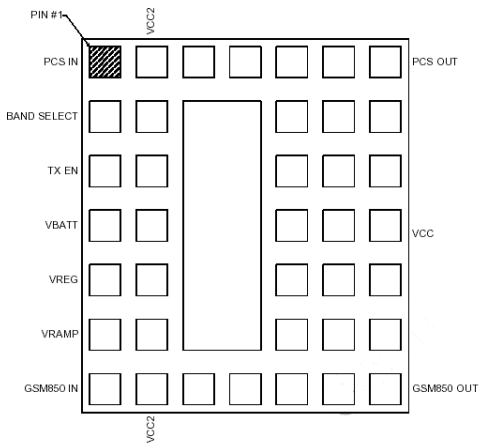
The required voltage BATT+ is provided by the battery.
The required voltage VREGRF2 for the power control circuit is provided by the ASIC D361.



Blockdiagram of R 340 (PA)



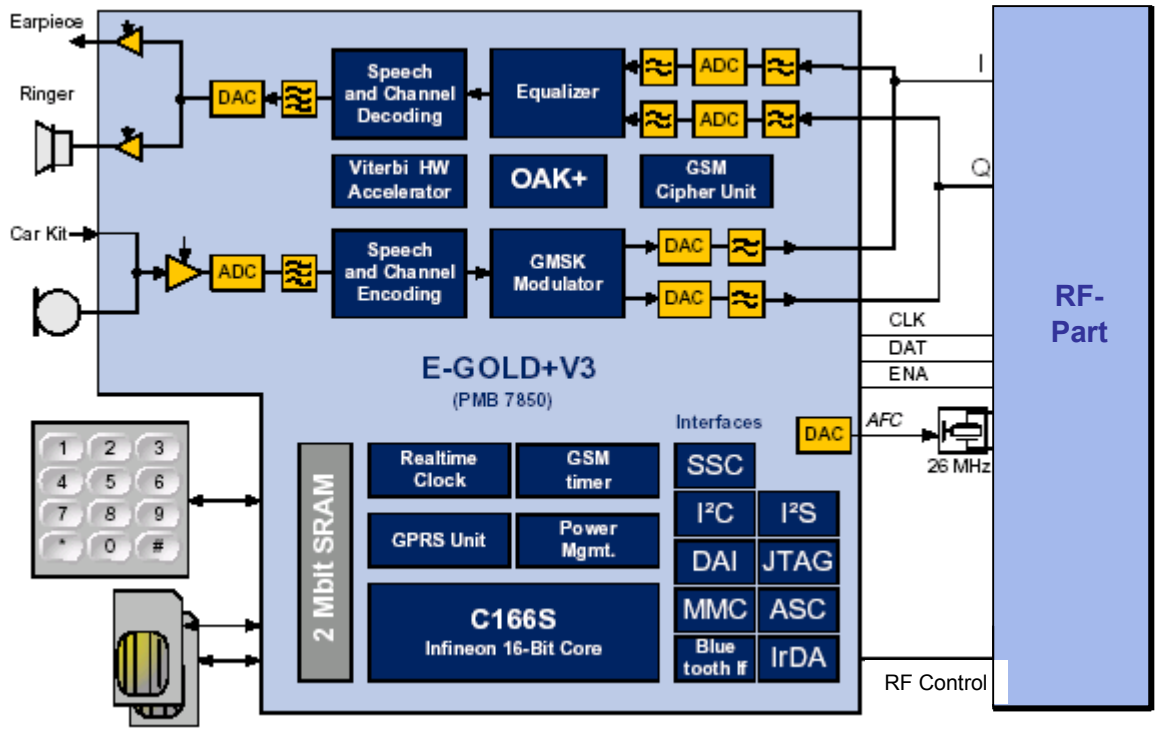
Pin Out



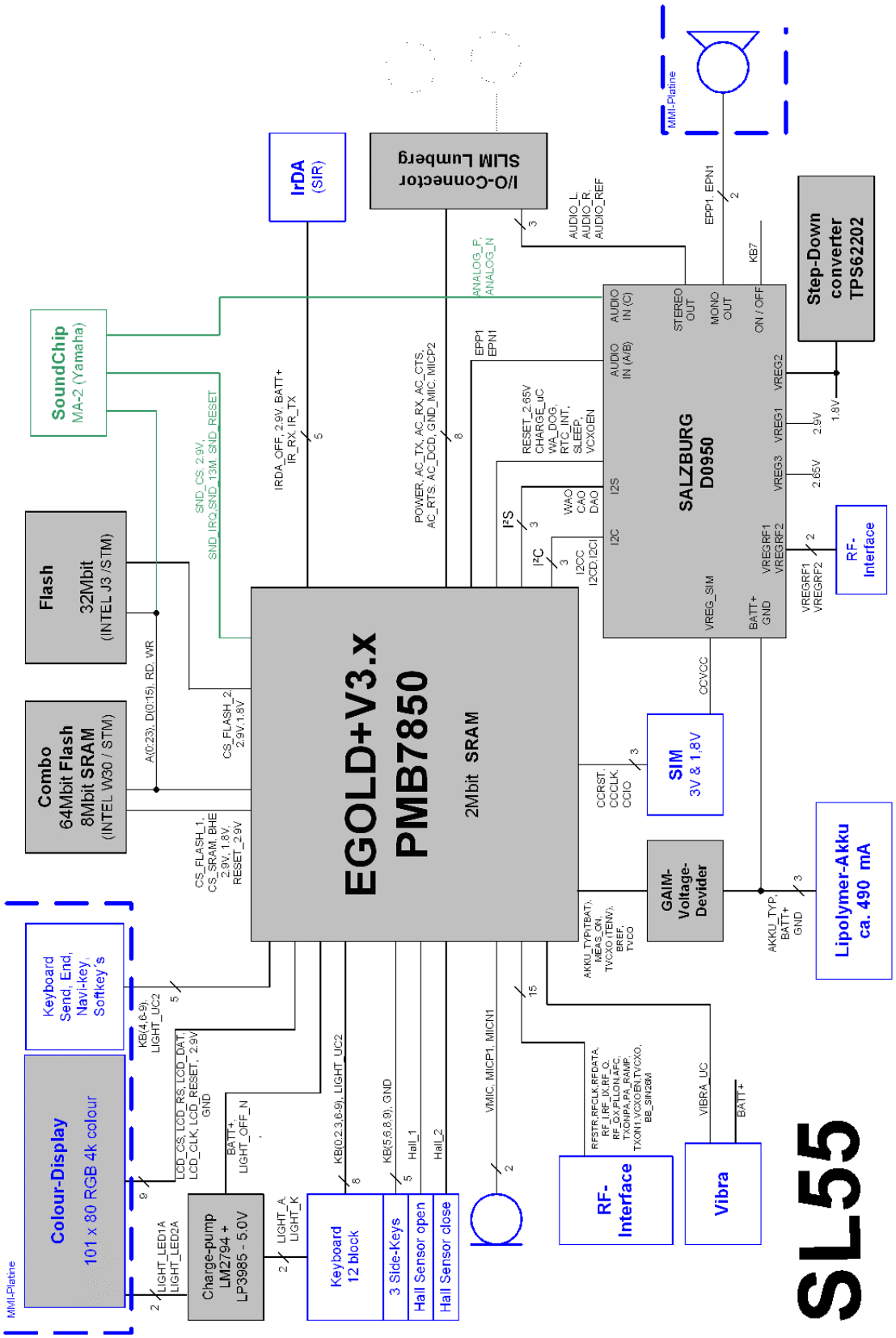
5 Logic / Control

5.1 Overview of Hardware Structure

5.1.1 Logic Block Diagram

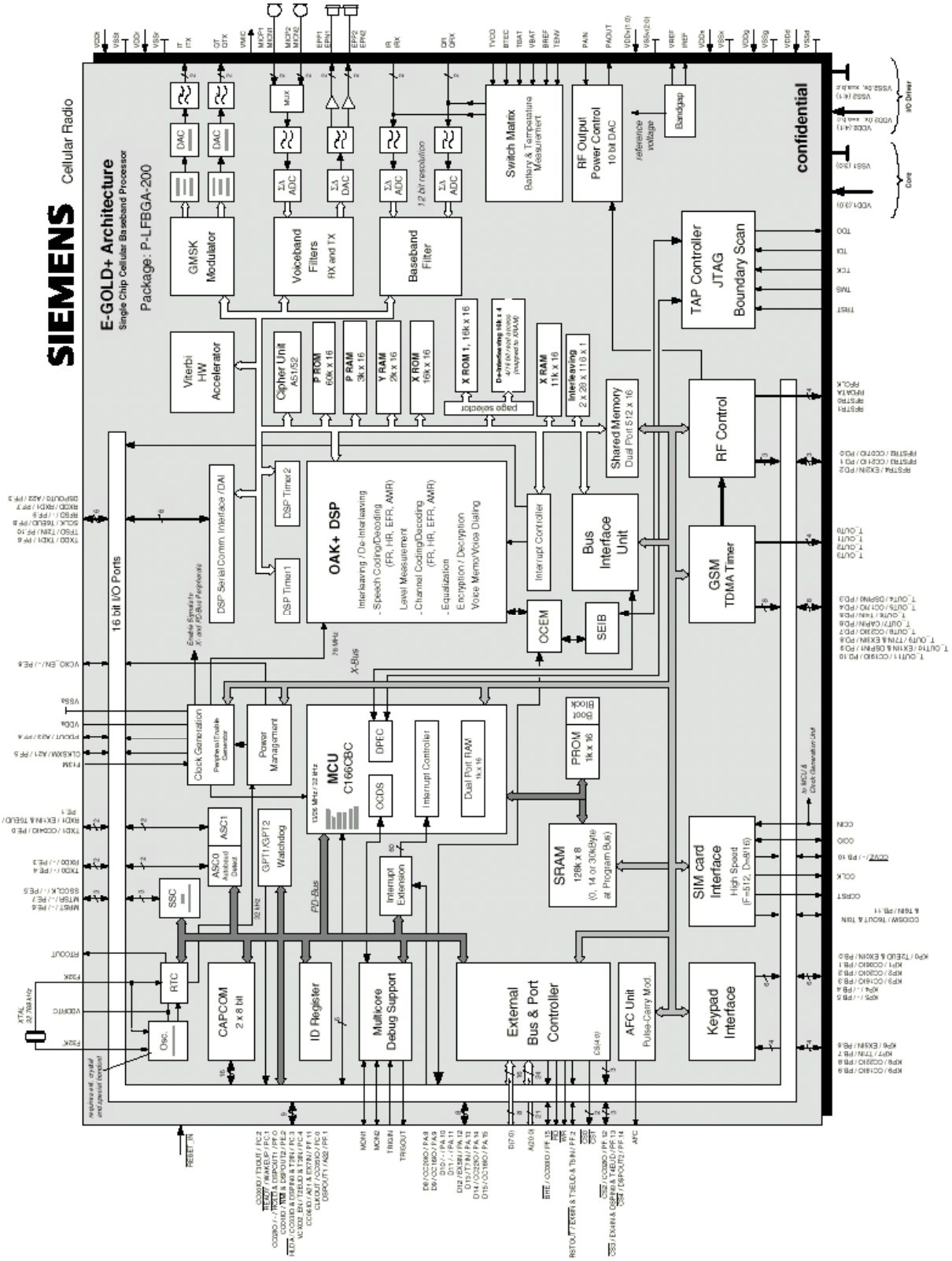


5.1.2 Block Diagram SL55 Control Part



5.1.3 EGOLD+

Block Diagram EGOLD+ V3.1



The EGOLD+ contains a 16-bit micro-controller (µC part), a GSM analog Interface (EGAIM), a DSP computing core (DSP part) and an interface for application-specific switch-functions.

The µC part consists of the following:

- Micro-controller
- System interfaces for internal and external peripheries
- On-chip peripheries and memory

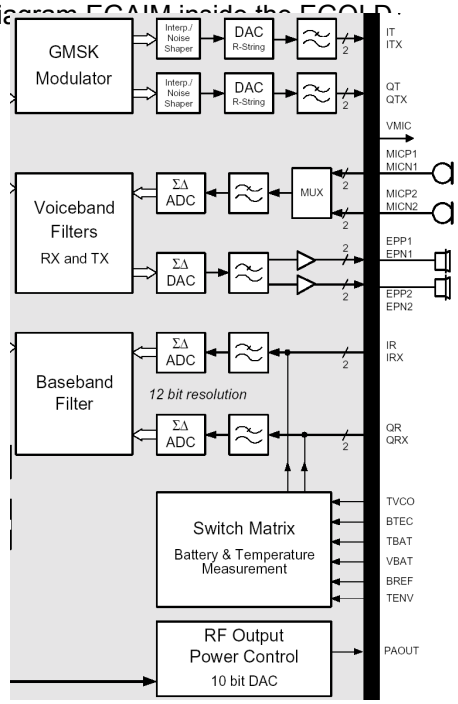
The Controller Firmware carries out the following functions:

- Control of the Man Machine Interface (keypad, LCD, sensing element, control of the illumination,...)
- GSM Layer 1,2,3 /GPRS
- Control of radio part (synthesizer, AGC, AFC, Transmitter, Receiver...),
- Control of base band processing (EGAIM)
- Central operating system functions (general functions, chip select logic, HW driver, control of mobile phones and accessories...).

The EGAIM part contains the interface between the digital and the analogue signal processing:

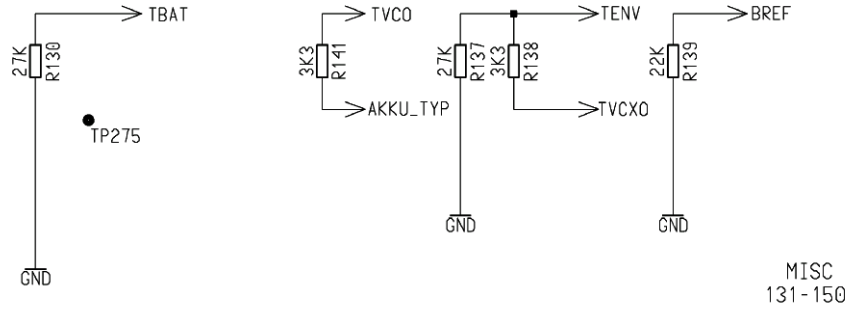
- 2 Sigma Delta A/D converters for RX signal, and for the necessary signals for the charge control and temperature measurement. For this, the converter inputs are switched over to the various signals via the multiplexer.
- 2 D/A converters for the GMSK-modulated TX signal,
- 1 D/A converter for the Power Ramping Signal,
- 1 Sigma Delta A/D and D/A converter for the linguistic signal.

Blockdiagram EGAIM inside the EGOLD+:



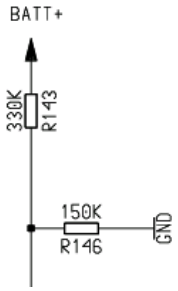
Measurement of Battery and Ambient Temperature

The battery temperature is measured via the voltage divider R1387, R138 by the EGOLD+ (Analog Interface P2). For this, the integrated ΣΔ converter of the RX-I base band branch is used. This ΣΔ converter compares the voltage of TBAT and TENV internally. Through an analogue multiplexer, either the RX-I base band signal, or the TBAT signal and the TENV signal is switched to the input of the converter. The signal MEAS_ON from the EGOLD+(GSM TDMA-TIMER H15) activates the battery voltage measurement The ambient temperature TENV is measured directly at of the EGOLD+ (Analog Interface P3).



Measurement of the Battery Voltage

The measurement of the battery voltage is done in the Q-branch of the EGOLD+, for this BATT+ is connected via a voltage divider R143, R146 to the EGOLD+(Analog Interface P1). An analogue multiplexer does the switching between the baseband signal processing and the voltage measurement.



A/D conversion of MIC-Path signals incl. coding

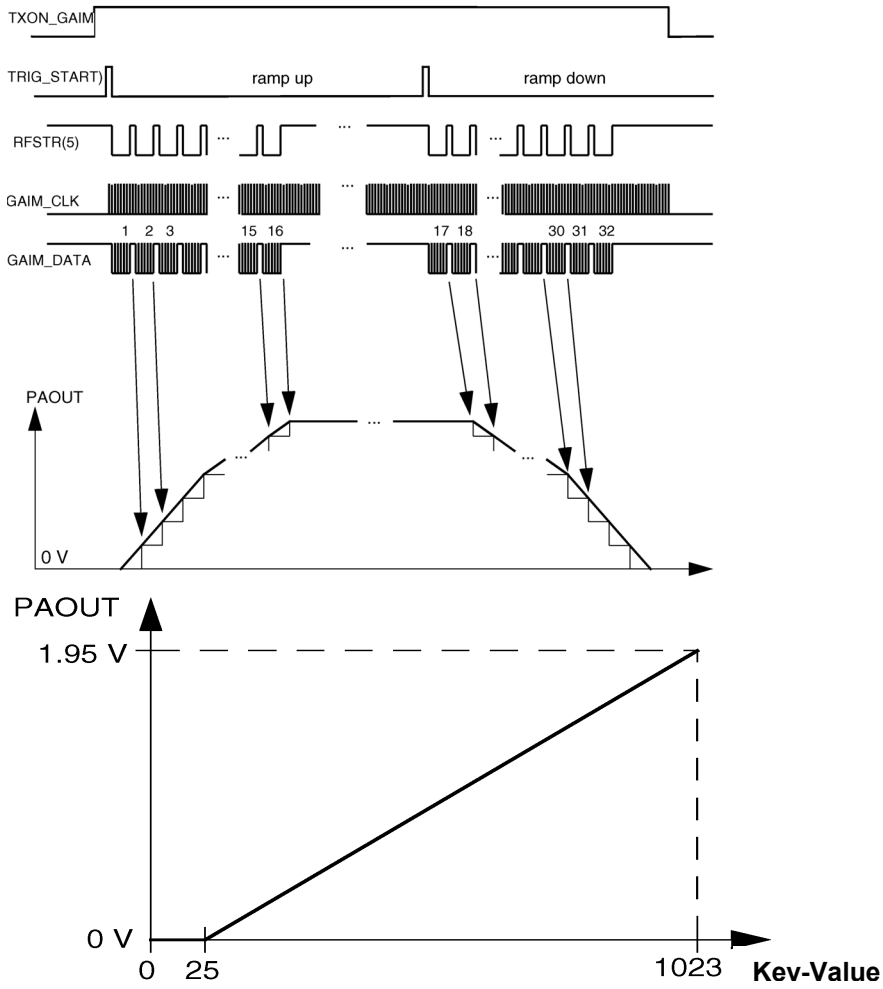
The Microphone signals (MICN2, MIP2, MICP1, MICN1) arrive at the voiceband part of the EGOLG+. For further operations the signals will be converted into digital information, filtered, coded and finally formed into the GMSK-Signal by the internal GMSK-Modulator. This so generated signals (RF_I, RF_IX, RF_Q, RF_QX) are given to the Bright IC in the transmitter path.

D/A conversion of EP-Path signals incl. decoding

Arriving at the baseband-Part, the demodulated signals (RF_I, RF_IX, RF_Q, RF_QX) will be filtered and A/D converted. In the voiceband part after decoding (with help of the µC part) and filtering, the signals will be D/A converted amplified and given as (EPP1_FIL, EPN1_FIL) to the Power Supply ASIC.

Generation of the PA Control Signal (PA_RAMP)

The RF output power amplifier needs an analogue ramp up/down control voltage. For this the EGOLD+ system interface generates 10 bit digital values which have to be transferred to the power ramping path. After loading into an 10 bit latch the signal will be converted into the corresponding analogue voltage (PA_RAMP) with a maximum of ~2V



The DSP part contains:

- DSP signal processor
- Separate program/data memory
- a hardware block for processing the RX signal,
- a hardware block for “ciphers“,
- a hardware block for processing the linguistic signal,
- a hardware block for the “GMSK modulator“,
- De-/ interleaving memory,
- Communication memory
- a PLL for processing and reproducing the VCXO pulse signal.

In the DSP Firmware are implemented the following functions:

- scanning of channels, i.e., measurement of the field strengths of neighbouring base stations
- detection and evaluation of Frequency Correction Bursts
- equalisation of Normal Bursts and Synchronisation Bursts
- channel encoding and soft-decision decoding for fullrate, enhanced-fullrate and adaptive multirate speech, fullrate and halfrate data and control channels.
- channel encoding for GPRS coding
- fullrate, enhanced fullrate and adaptive multirate speech encoding and decoding
- mandatory sub-functions like
  – discontinuous transmission, DTX
  – voice activity detection
  – background noise calculation
- generation of tone and side tone
- hands-free functions
- support for voice memo
- support for voice dialling
- loop-back to GSM functions
- GSM Transparent Data Services and Transparent Fax
- calculation of the Frame Check Sequence for a RLP frame used for GSM NonTransparent Data Services
- support of the GSM ciphering algorithm

Real Time Clock (integrated in the EGOLD+):
The real time clock is powered via a separate voltage regulator inside the Power Supply ASIC (D361 pin A5). Via a capacitor C374, data are kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with the possibility to switch the phone on.

5.1.4 SRAM

Memory for volatile data

Memory Size:	8 Mbit + 2Mbit SRAM internal EGOLD+ V3.1
Data Bus:	16Bit

5.1.5 FLASH

Memory Size:	64Mbit (8 Mbyte)
Data Bus:	16 Bit

5.1.6 SIM

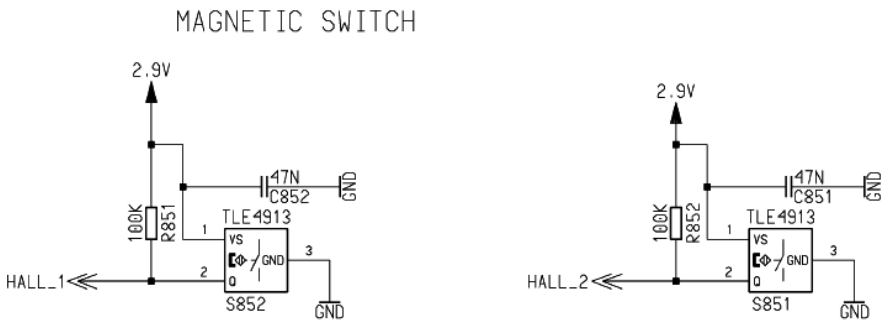
SIM cards with supply voltages of 1.8V and 3V are supported.

5.1.7 Vibration Motor

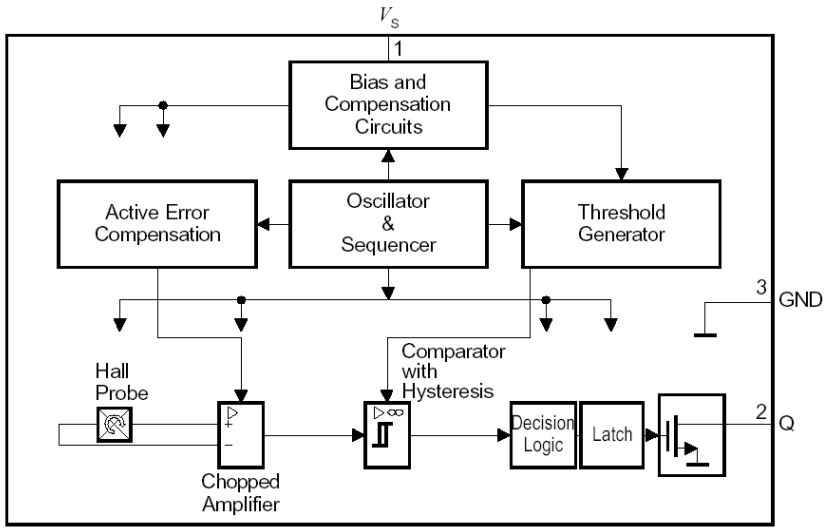
The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with spring contacts.

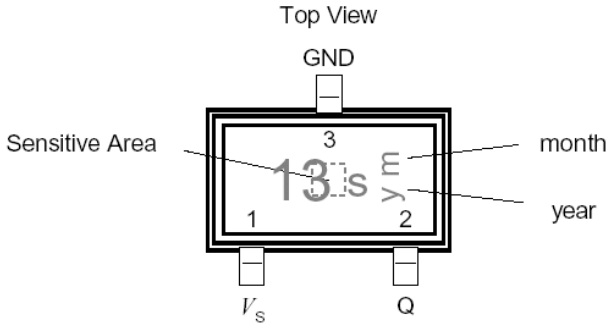
5.1.8 Hall sensor + magnet

To identify the position of the slider 2 Hall-sensors are placed on the PCB and 1 Magnet in the upper case. The sensor S852 detects the lower position of the slider, the signal HALL_1 in connected to the EGOLD+ (GSM TDMA Timer G17). The upper position of the slider is detected with S851with the signal HALL_2 (EGOLD+ (Serial Interface P15)).



Block diagram Hall-sensors





6 Power Supply

6.1 Power Supply ASIC

The power supply ASIC contains the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the µC with a watchdog
- Voltage regulator
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI interface
- I2C interface
- RC Oscillator
- Audio multiplexer
- Audio amplifier stereo/mono
- 18 bit Sigma/Delta DAC with Clock recovery
- Bandgap reference*

INFO:

*** Bandgap reference**

The p-n junction of a semiconductor has a bandgap-voltage. This bandgap-voltage is almost independent of changes in the supply voltage and has a very low temperature gradient. The bandgap-voltage is used as reference for the voltage regulators.

To reduce the power consumption of the ASIC and to ensure high efficiency of the power management concept a DCDC Converter N361 for the Core (EGOLD+V3X Baseband Chipset), Flash and SRAM supply is used. During this time all voltage regulators inside the ASIC are switched off.

The DCDC converter N361 includes the following functions:

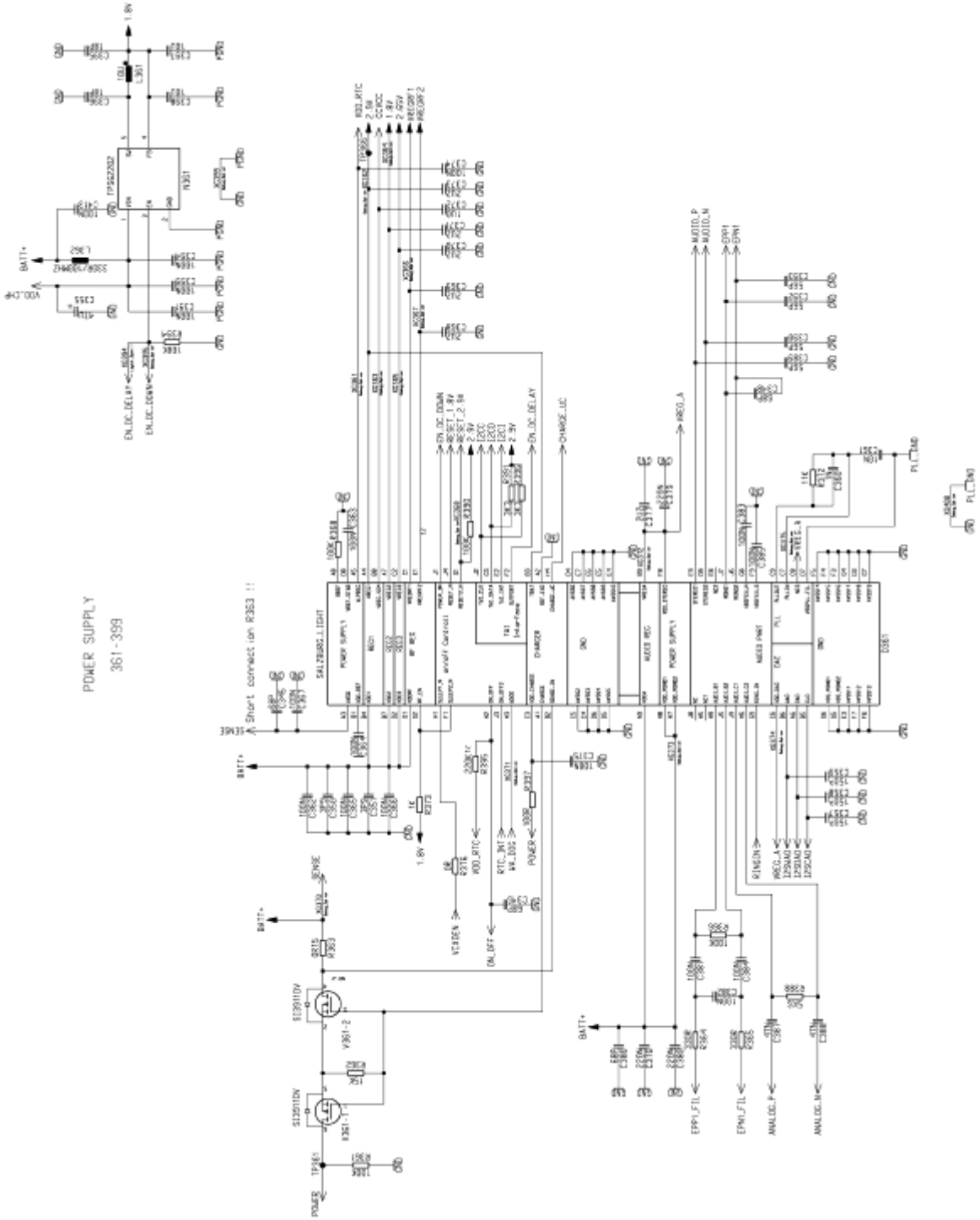
- PFM Mode for sleep mode of the Mobile Phone.
- PWM Mode for active mode of the Mobile Phone.

The mode change is controlled by the ASIC with the signal EN_DC_DOWN (Pin J1) based on the EGOLD+ signal VCXO_EN.

6.1.1 Pinout diagram

9	8	7	6	5	4	3	2	1	
Vdda	rref	vreg2	dao	vlpreg	vreg1	avdd	ref_exe	charge	A
vrega	vregsim	vdd2	wao	clo	vdd1	tbat	sense_in	vddref	B
pllout	vddpll	pllin	Vdddac	VSS	VSS	vdd_charge	vreg3	vregrf1	C
stereoL	vref_stab	VSSPLL	VSS	VSS	VSS	VSSSTAB	vdd3	vddrf	D
stereoR	stereom	VSS	VSS	VSS	VSS	VSS	twi_int	vregrf2	E
Vrefex_s	vddstereo	VSS	VSS	VSS	VSS	VSS	outport	sleep2_n	F
ringin	vrefex_m	VSSLNB	VSS	VSS	VSS	twi_data	rf_en	reset2_n	G
audiob1	vddmono1	vddmono2	audioc2	hv_fuse	charge_uc	wdog_uc	on_off	sleep1_n	H
audioc1	~~audioa1~~	mono1	mono2	audiob2	reset_n	on_off2	twi_clk	power_on	I

6.1.2 Power Supply Diagram



6.1.3 Power Supply Operating mode:

- **Power Down Mode** (mobile is switched off)
In power down mode the current consumption is very low. The inputs for switch on conditions (ON/OFF PinH2, ON/OFF2 PinJ3, VDD_CHARGE PinC3), the LPREG with his own voltage reference and POR cells are active. All other blocks are switched off, so the battery discharging will be kept to a minimum. This is the state when the phone is switched off.

- **Start Up Mode** (user switch on, RTC switch on)
"Start Up Mode" can be initiated by ON_OFF (falling edge) or ON_OFF2 (rising edge). In this mode a sequential start-up, of reference oscillator, voltage supervision and regulators is controlled by digital part. In case of failure (overvoltage or time out of the µC reaction), the ASIC shuts down.

-**Trickle Charge Mode** (to be able to charge the battery)
In case of a rising edge at VDD_CHARGE, the ASIC switches from power down to an interim state. In this state, the oscillator and the reference are started. If the voltage on VDD_CHARGE is below the charger detection threshold, the ASIC shuts off. If the voltage on VDD_CHARGE is high enough the signal EXT_PWR is going to H and the power up continues. Depending on the voltage of the battery an initial charging of the battery of the circuit is immediately done. If the Trickle Charge Mode is entered with a very low battery, the supply for the ASIC itself is generated from the internal VDDREF regulator. If a failure is detected (overvoltage), the ASIC is switched off.

- **Normal Mode** (following Start Up Mode or Trickle Charge Mode)
The normal mode is the situation, where the startup has been finished and the ASIC starts the external µC by changing the signal RESETN from low to high.
Mode: a) Active Mode with full capabilities of all blocks
b) Sleep Mode with reduced capabilities of some blocks and some even not available at all.

-**Active Mode** (submode of Normal Mode)
In this mode, the µC controls the charging block and most of the failure cases. The ASIC can be controlled by the TWI interface, interrupt request can be sent by the ASIC. Furthermore, the voltages are supervised (in case of failure the µC will be informed). In case of watchdog failure, overvoltage or power on request, the ASIC will be switched off immediately. The mono and the stereo block can be switched on in active mode.

-**Sleep Mode** (submode of Normal Mode)
Intention of the mode is to have limited functions available, with a reduced current consumption. A low level at the pin SLEEP1_N will switch from Active Mode to Sleep Mode. In Sleep Mode all charging functions and supply overvoltage detection are switched off. LDO undervoltage detection, clock and reference voltages are active. LDOs are working in low current mode. The battery voltage comparators are available, the audio block can be switched on.

6.1.4 Power Supply Functions:

- **Power on Reset**

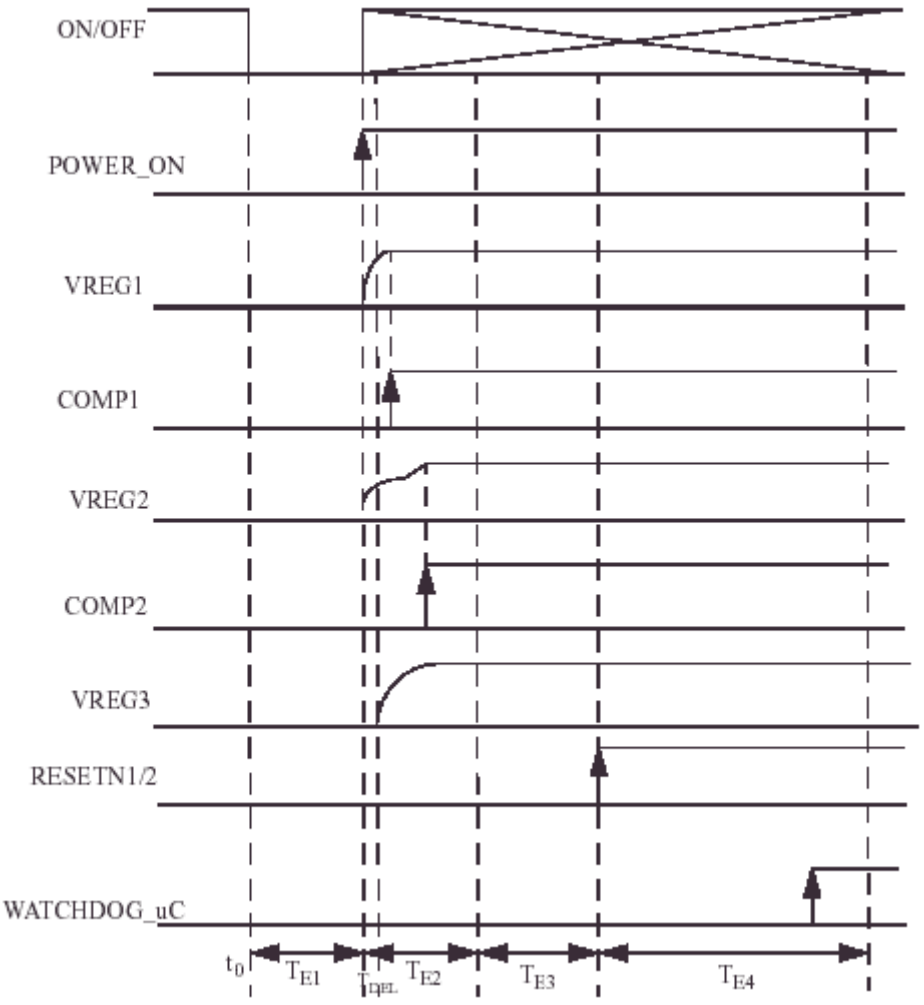
To guarantee a defined startup, the ASIC will be reset by a Power on Reset block. After Power on Reset the ASIC will enter the power done Mode. If the thresholds will be reached during operating mode the reset will become the device enters the power down mode. This blocks are always active and will be supplied by VDDREF.

- **Switch on and watchdog**

There are 3 different possibilities to switch on the phone via external pins:

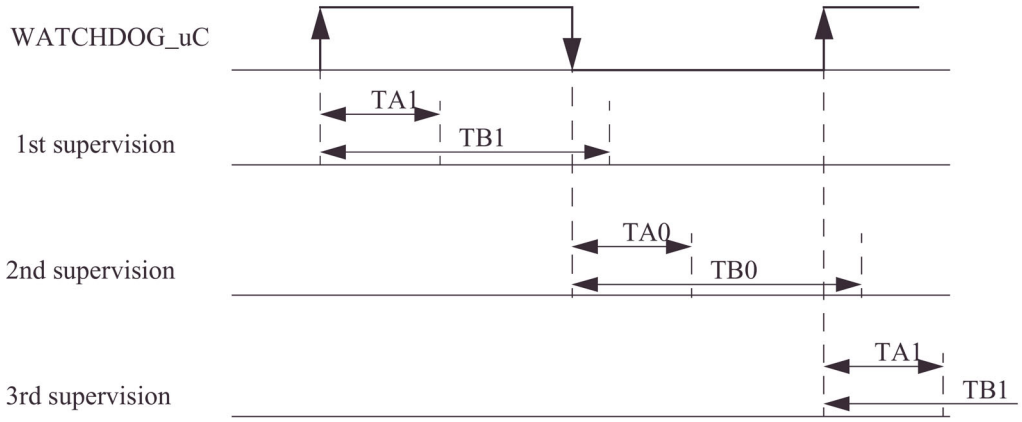
-VDD_CHARGE with rising edge
-ON/OFF with falling edge
-ON/OFF2 with rising edge

In order to guarantee a defined start-up behavior of the external components, a sequential power up is used and the correct start up of blocks is supervised. In normal mode, a continues watchdog signal from the µC is needed to keep the system running. If this signals fails, the ASIC will switch to power down mode.
It must be guaranteed, that each start up condition does not interfere and block the other possible start up signals. In case of failure during start up, the device will go back to power down mode. To guarantee that the connection of the a charging unit with a very low battery is detected, this detection must work level sensitive at the end of POR signal.



- **Watchdog monitoring**

As soon as the first Watchdog_µC signal with a rising edge is detected , the ASIC starts the watchdog monitoring procedure. Standard switch off of the phone is the watchdog. The first edge of watchdog is rising. If a falling edge is detected ass the first transient the device will go to power down mode again and the whole phone is switched off.



Rising and falling edges must be detected alternated. With any edge of the Watchdog_µC signal a counter will be reseted. The next – compared to the previous edge – inverted edge must occur between end of TA0,TA1 and end of TB0,TB1. If the signal occurs before end of TA0, TA1 or is not detected until end of TB0, TB1, the device will go to power down mode immediately after the violation of the WD criteria occurs.

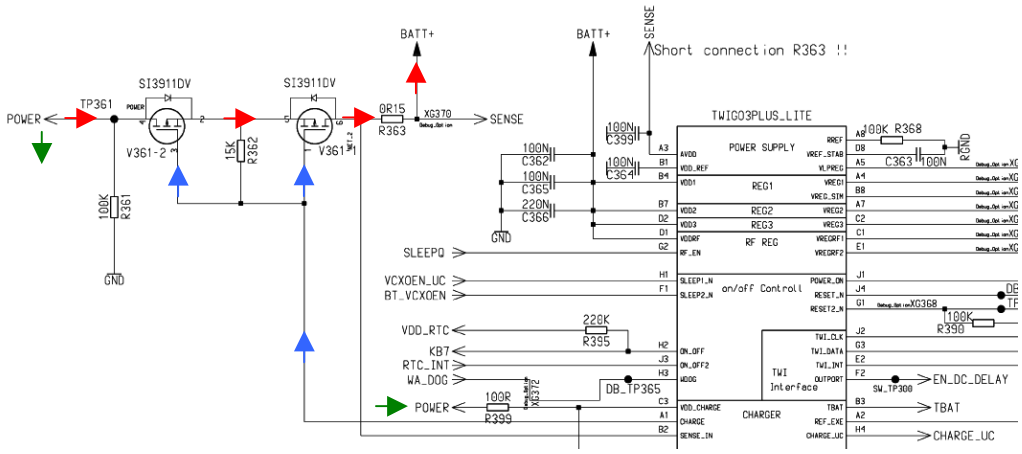
TA0, TA1 ~ 0.4 sec
TB0, TB1 ~ 3 sec

6.2 Battery

As a standard battery a LiIon battery with a nominal capacity of 3,7 Volt/700mAh is used.

6.3 Charging Concept

Charging current
Charging control signal
Operating voltage for Trickle charge



6.3.1.1 Charging Concept

General

The battery is charged in the unit itself. The hardware and software is designed for LiIon with 4.2V technology.
Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging takes place in the background (the customer can see this via the “Charge” symbol in the display). During normal use the phone is being charged (restrictions: see below).
Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The EGOLD+ takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the POWER SUPPLY ASIC hardware can override/interrupt the charging in the case of over voltage of the battery (only for Manganese Chemistry Battery types e.g. NEC).
With the new slim Lumberg IO connector the charger recognition via SB line is lost. Now the charge current is measured inside the POWER SUPPLY ASIC with a current monitor.
The charging software is able to charge the battery with an input current within the range of 350-600mA. If the Charge-FET is switched off, no charging current will flow into the battery (exception is trickle charging, see below).
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. The NTC for the ambient temperature will be on the PCB (26 MHz part).

Two Wire Interface (TWI):

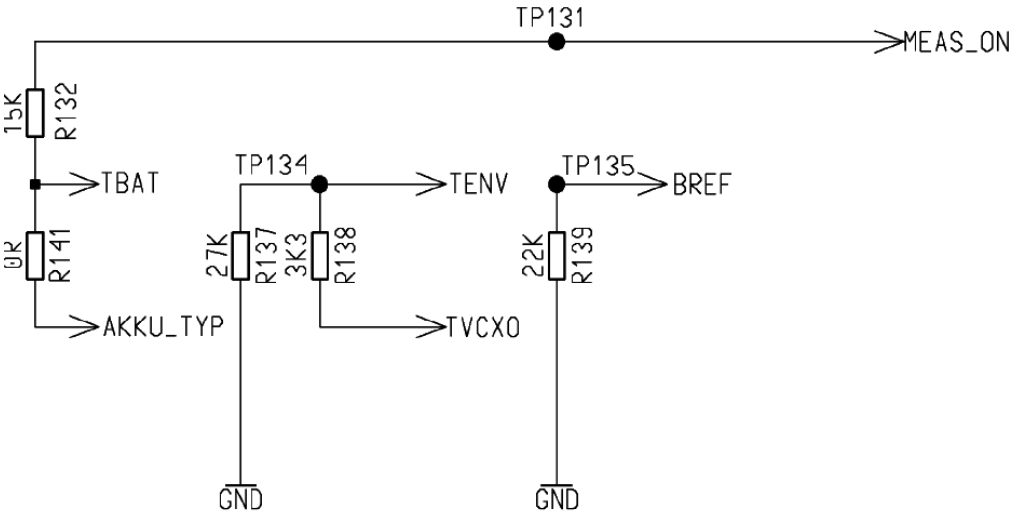
The TWI bus interface in configured as a slave unit with 1bit INT (interrupt), 1 bit SDA (serial data) and 1 bit SCL (serial clock). The data and the address of the register files are defined including read/write bit, control status bits(like ON/OFF, EXT_PWR, CHARGE...). The TWI interface is asynchronous with the internal clock. The TWI interface is reset with POR condition or falling edge of RESETN signal.

Measurement of, Battery Type and Battery/Ambient Temperature

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the EGOLD. For this, the integrated ΣΔ converter in the EGOLD of the RX-I base band branch will be used. Via an analogue multiplexer, either the RX-I base band signal, the battery code voltage or the ambient temperature voltage can be switched over to the input of the converter. The 1-Bit data stream of the converter will be subjected to a data reduction via the DSP circuit so that the measured voltage (for battery and ambient temperature) will be available at the end as a 10-bit data word.

Measurement of the Battery Voltage

Analogue to the I-branch either the RX-Q base band signal or the battery voltage can be measured in the Q-branch. Processing in the DSP circuit will be done analogue to the I-branch. The EGOLD will be specified internally at voltage measurement input BATT+ for an input voltage of 3V...4.5V.



Timing of the Battery Voltage Measurement
Unless the battery is charging, the measurement is made in the TX time slot. During charging it will be done after the TX time slot. At the same time, either the battery temperature (in the I-branch) and the battery voltage (in the Q-branch) or the ambient temperature in the I-branch can be measured (the possibility of measurement in the Q-branch, the analogue evaluation of the battery coding, is used for HW-Coding). Other combinations are not possible. For the time of the measurement the multiplexer in the EGAIM must be programmed to the corresponding measurement.

Recognition of the Battery Type
The battery code is a resistor with a resistance depending on the manufacturer.

Charging Characteristic of Lithium-Ion Cells
LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is approx. 600mA, minimum about 100mA. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be started ranges from 5...40°C, and the temperature at which charging takes place is from 0...45°C. Outside this range no charging takes place, the battery only supplies current.

Trickle Charging
The POWER SUPPLY ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the POWER SUPPLY ASIC. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.75V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the POWER SUPPLY ASIC will switch on the phone automatically and normal charging will be initiated by software (note the restrictions on this item as stated below).

Normal Charging
For battery voltages above 3.2 Volt and normal ambient temperature between 5 and 40°C the battery can be charged with a charge current up to 1C*. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the POWER SUPPLY ASIC. The level of charge current is limited/controlled by the accessory or charger.

USB Charging
For battery voltages above 3.2 Volt and normal Temperature between 5 and 40°C the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) with a supply voltage between 3.6 and 5.4 Volt is detected by the POWER SUPPLY ASIC during active mode of the phone. To enable this charging mode, the mobile phone must be registered (logged on) to a USB Host. The Charge-Only and Trickle-Charge Mode is not supported because of USB Spec. restrictions. The charge current is controlled by the POWER SUPPLY ASIC.

INFO:

*** C-rate**

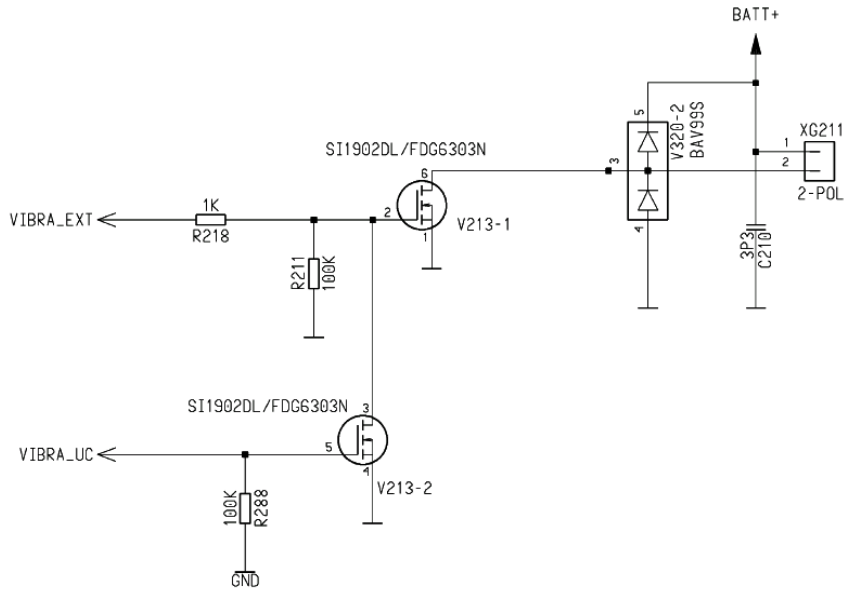
The charge and discharge current of a battery is measured in C-rate. Most portable batteries, are discharge with 1C. A discharge of 1C draws a current equal to the battery capacity. For example, a battery value of 1000mAh provides 1000mA for one hour if discharged at 1C. The same battery discharged at 0.5C provides 500mAfor two hours. At 2C, the same battery delivers 2000mA for 30 minutes. 1C is often referred to as a one-hour discharge; a 0.5 would be a two-hour, and a 0.1C a 10 hour discharge.

Restrictions

- A battery which has completely run down can not be re-charged quickly because the battery voltage is less than 3.0V and the logic which implements the charge control cannot be operated at this low voltage level. In this case the battery is recharged via trickle-charging. However, the charging symbol cannot be shown in the display because at this time logic supply voltages are not operating. The charging time for this trickle-charging (until the battery can be fast-charged from then on) is in the range of 1 hour. If, within this time, the battery voltage exceeds 3.2V, then the POWER SUPPLY ASIC switches on the mobile and charging continues in the Charge-Only Mode. In some circumstances it can happen that after trickle-charging and the usually initiated switch-on procedure of the mobile, the supply voltage collapses so much that the mobile phone switches off again. In this case trickle charging starts again with a now raised threshold voltage of 3.75V instead of 3.2V, at maximum for 20 minutes. The POWER SUPPLY ASIC will retry switching on the phone up to 3 times (within 60 minutes overall).
- Charging the battery will not be fully supported in case of using old accessory (generation '45' or earlier). It is not recommended to use any cables that adapt "old" to "new" Lumberg connector. Using such adapters with Marlin will have at least the following impact:
  1) half-sine wave chargers (e.g. P35 & home station) can not be used for trickle charging
  2) normal charging might be aborted before the battery is fully charged
  3) EMC compliance can not be guaranteed
- A phone with a fully charged LiIon battery will not be charged immediately after switch-on. Any input current would cause an increase of the battery voltage above the maximum permissible value. As soon as the battery has been discharged to a level of about 95% (due to current consumption while use), it will be re-charged in normal charging mode.
- The phone cannot be operated without a battery.
- The phone will be destroyed if the battery is inserted with reversed polarity:
- ⇒ design-wise it is impossible to wrongly pole the phone. This is prevented by mechanical means.
- ⇒ electrically, a correctly poled battery is presumed, i.e. correct polarity must be guaranteed by suitable QA measures at the supplier
- The mobile phone might be destroyed by connecting an unsuitable charger:
- ⇒ a charger voltage >15V can destroy resistances or capacitors
- ⇒ a charger voltage >20V can destroy the switch transistor of the charging circuit
  In case the transistor fails the ASIC will be destroyed. In the case of voltages lower than 15V and an improper current limitation the battery might be permanently damaged. A protection against grossly negligent use by the customer (e.g. direct connection of the charge contact to the electricity supply in a motor car) is not provided. Customer safety will not be affected by this restriction.

7 Interfaces

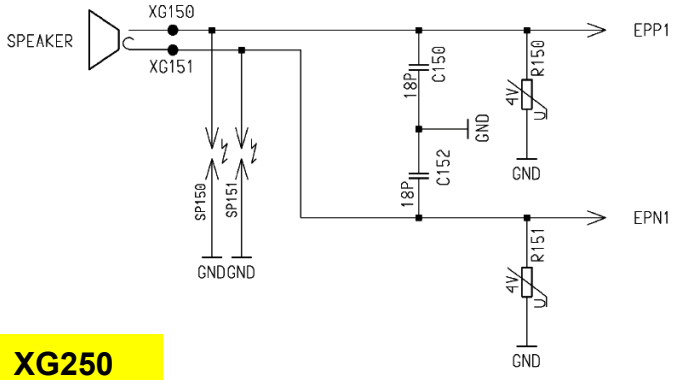
7.1 Vibra



XG211

Pin	IN/OUT	Remarks
1	I	2.9V
2	O	The FET V213, switching this signal, is controlled via the EGOLD+ signal VIBRA_UC and via the Soundchip signal VIBRA_EXT.

7.2 Earpiece

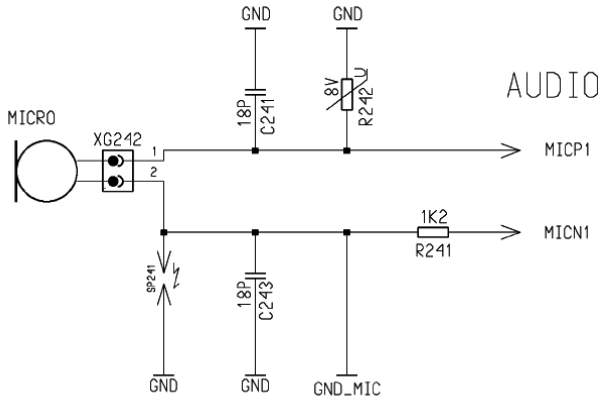


XG250

Pin	Name	IN/OUT	Remarks
1	EPP1	O	1st connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. EPP1 builds together with EPN1 the differential output to drive the multifunctional “earpiece” (earpiece, ringer, handsfree function).

Pin	Name	IN/OUT	Remarks
2	EPN1	O	2nd connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation.

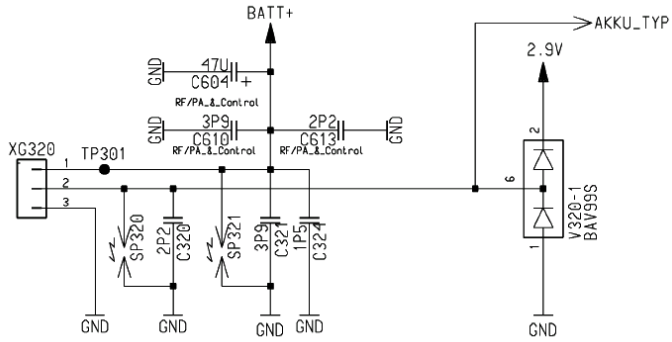
7.3 Microphone



XG242

Pin	Name	IN/OUT	Remarks
1	MICP1	I	Speech signal. The same line carries the microphone power supply.
2	MICN!/GND_MIC		

7.4 Battery

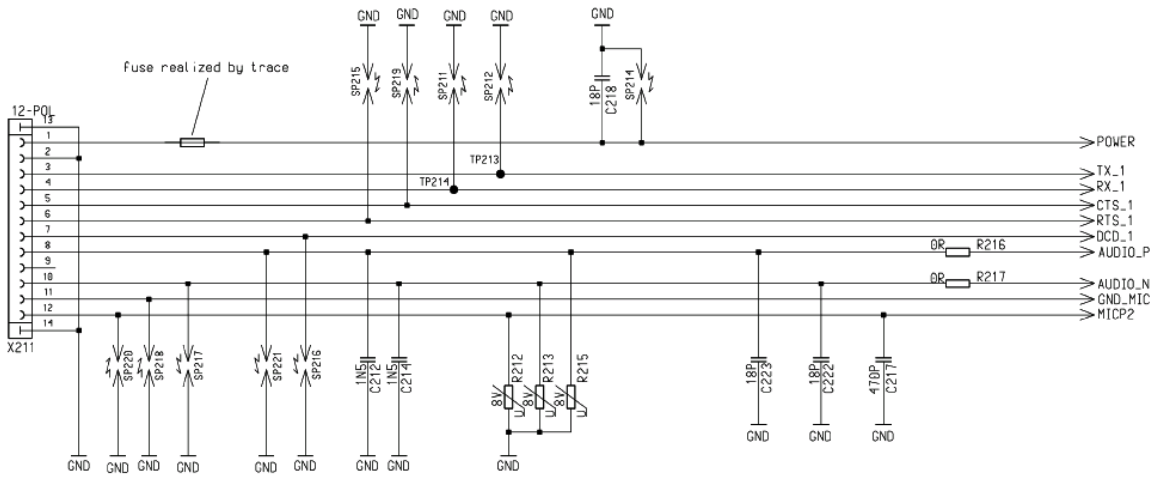


XG181

Pin	Name	Level	Remarks
1	BATT+	3 V... 4.5V	Positive battery pole
2	AKKU_TYP	0V...2.65V	Recognition of battery/supplier
3	GND		Ground

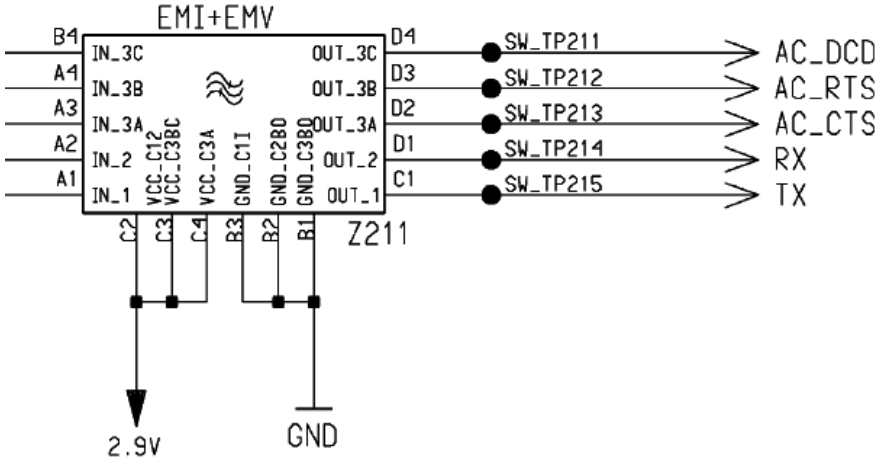
7.5 IO Connector with ESD protection

7.5.1 IO Connector – New Slim Lumberg



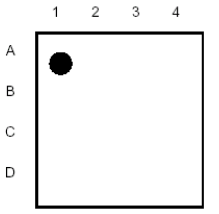
Pin	Name	IN/OUT	Notes
1	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
2	GND		
3	TX	O	Serial interface
4	RX	I	Serial interface
5	DATA/CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
6	RTS	I/O	Use as RTS in data-operation.
7	CLK/DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
8	AUDIO_L	Analog O	driving ext. left speaker With mono-headset Audio_L and Audio_R differential mode
9			
10	AUDIO_R	Analog O	driving ext. right speaker With mono-headset Audio_L and Audio_R differential Signal
11	GND_MIC	Analog I	for ext. microphone
12	MICP2	Analog I	External microphone

7.5.2 ESD Protection with EMI filter



The Z211 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z211 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages up to 8 kV.

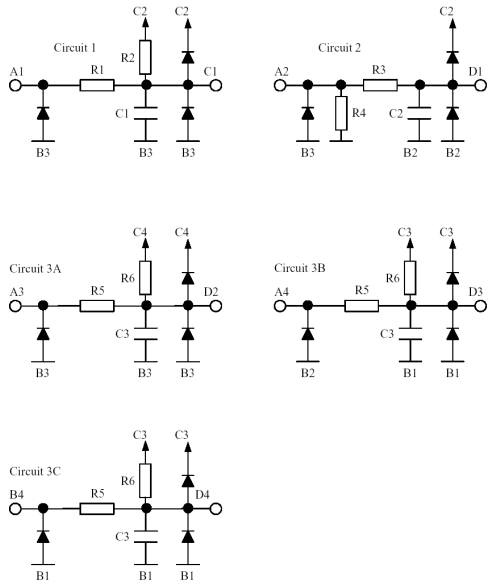
Pin configuration of the Z211



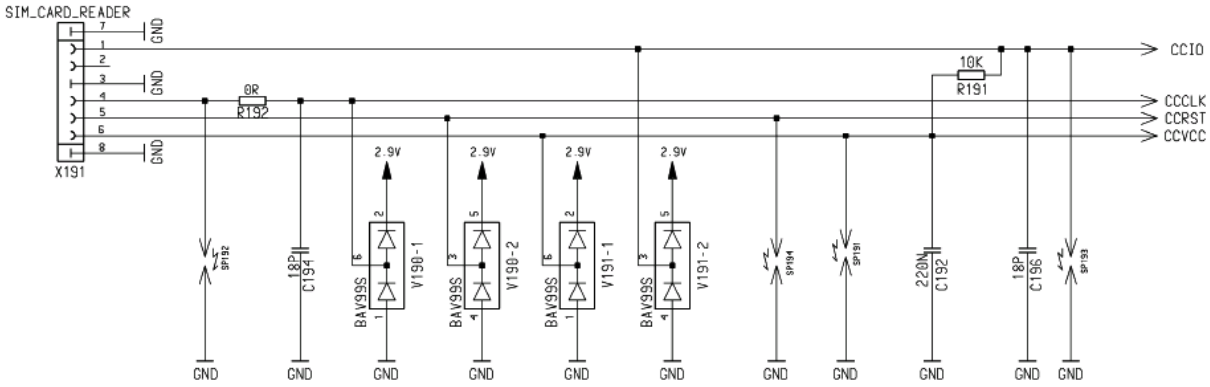
Top View (Bumps down)

PIN	DESCRIPTION	PIN	DESCRIPTION
A1	Input Circuit 1	C1	Output Circuit 1
A2	Input Circuit 2	C2	Vcc C1/C2
A3	Input Circuit 3A	C3	Vcc C3B/C3C
A4	Input Circuit 3B	C4	Vcc C3A
B1	GND C3Bo/C3Ci/C3Co	D1	Output Circuit 2
B2	GND C2o/C3Bi	D2	Output Circuit 3A
B3	GND C1i/C1o/C2i/C3Ai/C3Ao	D3	Output Circuit 3B
B4	Input Circuit 3C	D4	Output Circuit 3C

Z211 Circuit Configuration

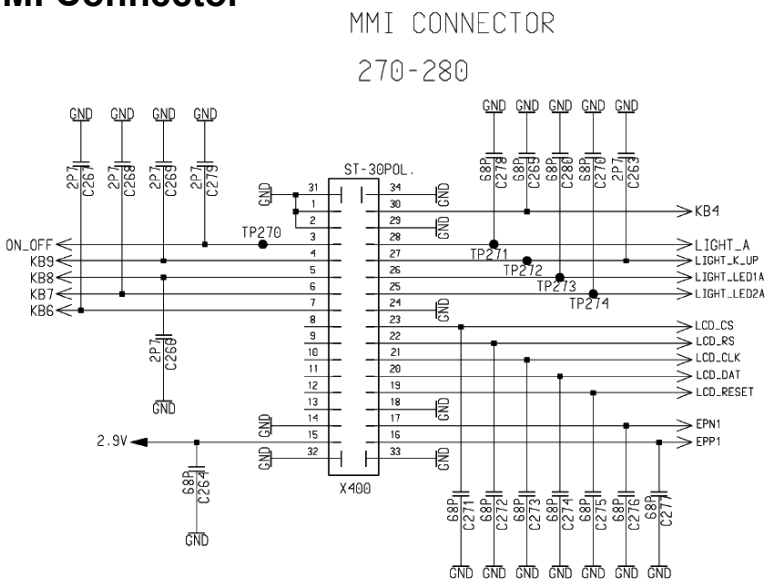


7.6 SIM



Pin	Name	IN/OUT	Remarks
1	CCVCC	-	Switchable power supply for chipcard; 220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes.
2	CCRST	O	Reset for chipcard
3	CCLK	O	Pulse for chipcard. The chipcard is controlled directly from the EGOLD+.
4			
5	GND		
6			
7	CCIO	I	Data pin for chipcard; 10 kΩ pull up at the CCVCC pin

7.7 MMI Connector



Pin	Name	Remarks
1	GND	GND
2	GND	GND
3	ON/OFF	ON/OFF key
4	KB9	Keyboard line 9
5	KB8	Keyboard line 8
6	KB7	Keyboard line 7
7	KB6	Keyboard line 6
8		
9		
10		
11		
12		
13		
14	GND	GND
15	2,9V	Power supply display controller
16	EPP1	Loudspeaker positive
17	EPN1	Loudspeaker negative
18	GND	GND
19	LCD_RESET	LCD Reset
20	LCD_DAT	LCD Data line
21	LCD_CLK	LCD Clock
22	LCD_RS	LCD Register select
23	LCD_CS	LCD Chip select
24	GND	GND
25	LCD_LED2A	Power supply display led 2
26	LCD_LED1A	Power supply display led 1
27	LIGHT_K_UP	Switched GND for display led 1 and led 2
28	LIGHT_A	Power supply display light
29	GND	GND
30	KB4	Keyboard line 4
31	GND	GND
32	GND	GND
33	GND	GND

Pin	Name	Remarks
34	GND	GND

8 Acoustic

The buzzer and the keypad clicks will be realized over the earpiece. At normal buzzer the signaling will realized with swelling tones. At the same time a maximum sound pressure level in the coupler of 135 +/- 5dB(A) is fixed.
The standard sounds will be generated by the EGOLD+, the advanced sounds will be generated via firmware running on the DSP.

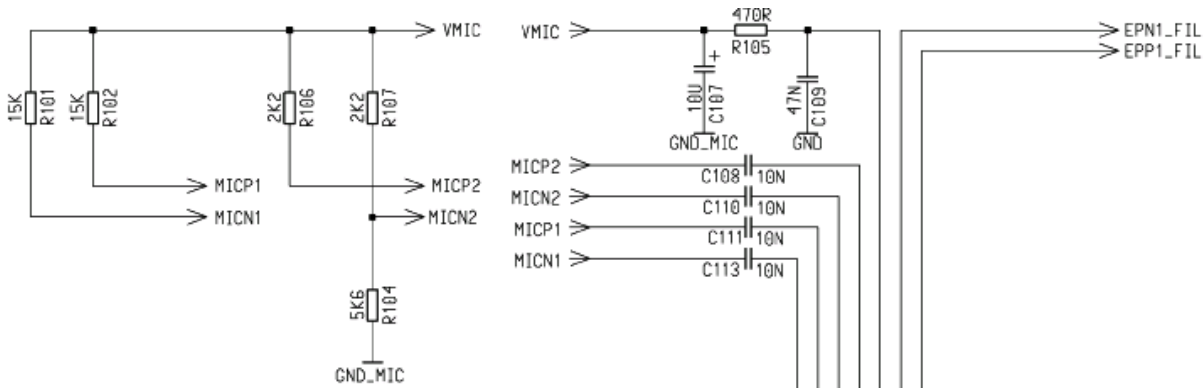
8.1 Microphone

8.1.1 Mechanical

The microphone is built in the Mounting Frame Lower Part and is mechanically fixed with a rubber seal (gasket). The contact on the PCB is realised via spiral springs, which are integrated in the gasket. Because of usage of Unidirectional Microphone, the gasket has a front- and a back sound-inlet hole. The front sound-inlet is acoustically tighten connected with a sound-inlet at the rear-side of the mounting frame lower part. The back sound-inlet is acoustically tighten connected with a sound-inlet at the bottom-side of the mounting frame lower part. The gasket of the microphone has a asymmetrical shape in order to provide non-rotating, guaranteed covering of the sound-inlets of mounting frame lower part to the corresponding sound-inlets at microphone gasket.

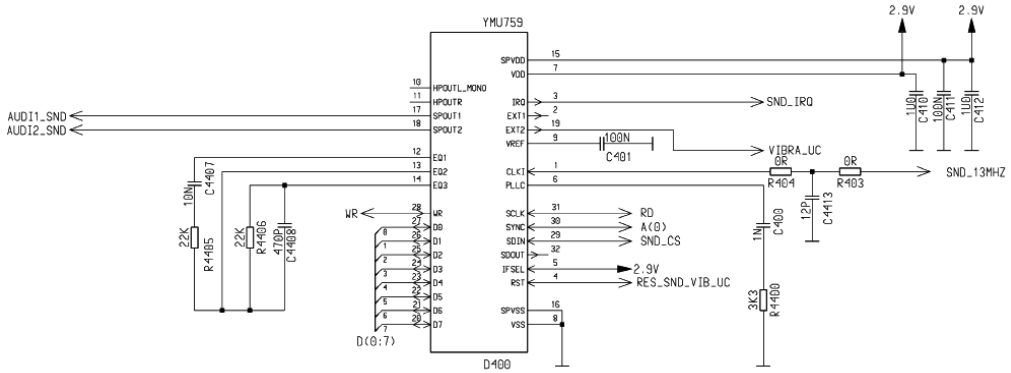
8.1.2 Electrical

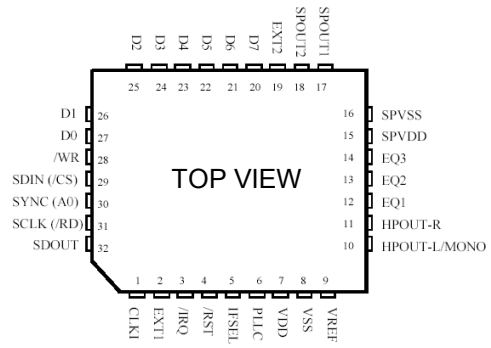
Both Microphones are directly connected to the EGOLD+.(Analog Interface G2, F1, G3, H2) via the signals MICN1, MICP1 (Internal Microphone)and MICN2, MICP2 (External Microphone/Headset). Power supply for the Microphone is VMIC (EGOLD+.(Analog Interface G1))



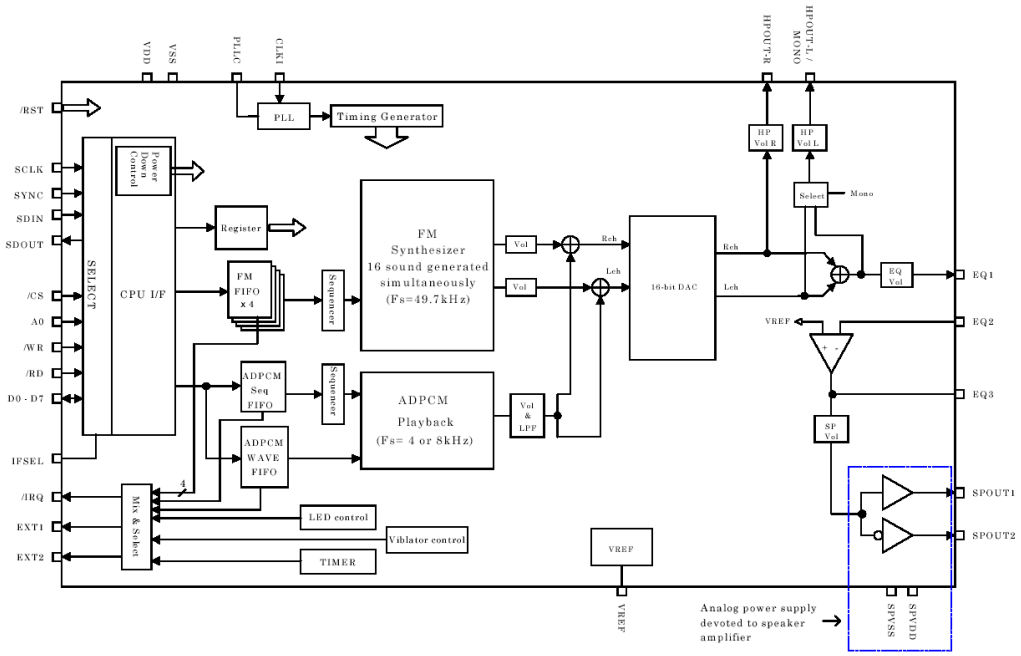
8.2 Soundchip

The D400 is used for Stereophonic Sound Generation. The internal CPU receives the data from the EGOLD+ via the address- and data- bus. Via a 16 sound FM synthesizer and DA converter the analogue output signal (AUDI1_SND, AUDI2_SND) goes to the audio amplifier inside the Power Supply ASIC. The clock for the D400 (SND_13MHZ/Miscellaneous U6) is made inside the EGOLD+, based of the 26MHZ VCO.





Blockdiagram



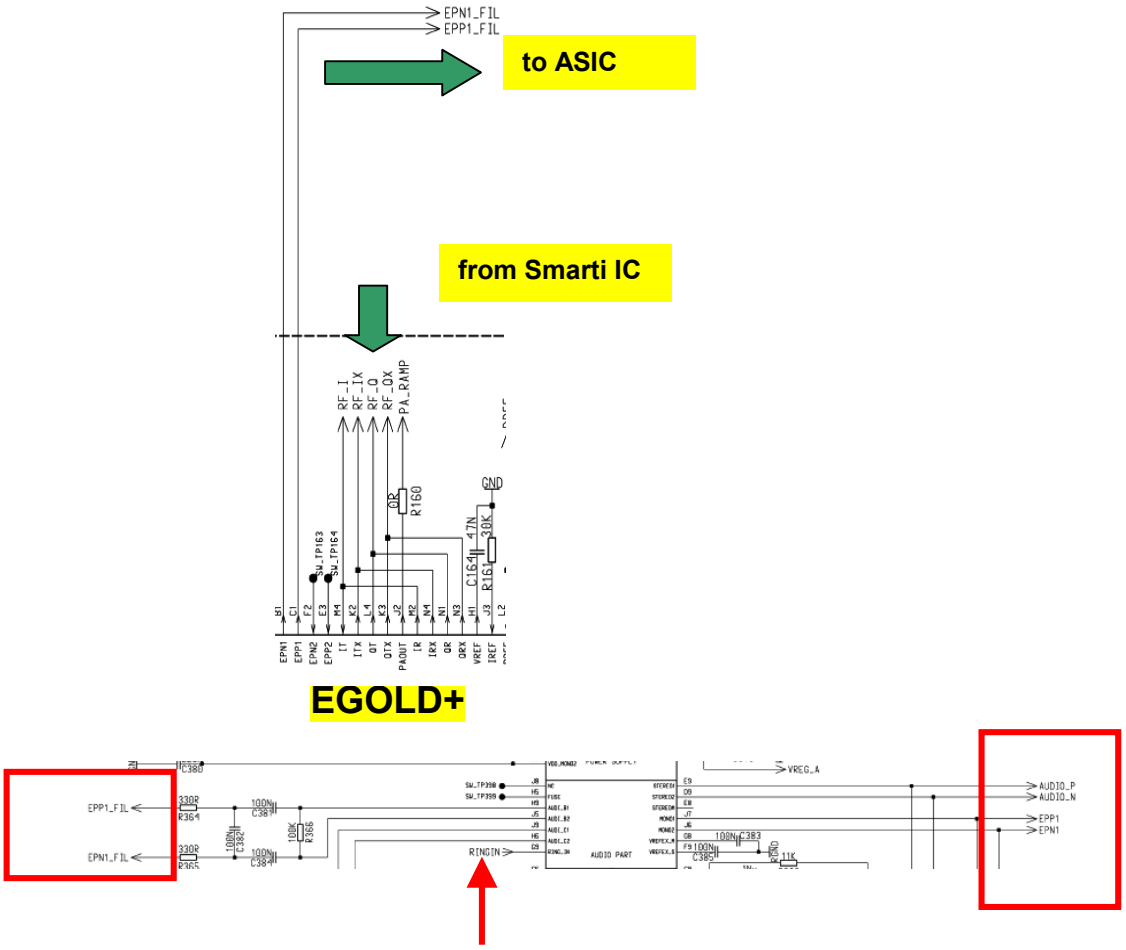
8.3 Earpiece/Loudspeaker

8.3.1 Mechanical

The speakermodule is designed to provide optimal performance for mobile handsfree and sound ringer. Plus independent from mobile leakage sound performance. Therefore speakermodule is a system that has a closed front volume with sound-outlets towards the ear of the user. Backvolume of Speakermodule is using the unused air between the antenna and the PCB. Backvolume is just used for resonance, there is no sound output from backvolume. The speakermodule is glued to the lightguide and contacted via two bending springs to the PCB. The lightguide itself is screwed with six screws via the PCB to the mounting frame lower part. Two of the six screws are located besides of the connection of speakermodule and lightguide. Therefore a good and reliable connection between speakermodule and PCB should be provided.

8.3.2 Electrical

The internal and external Loudspeaker (Earpiece) is connected to the voiceband part of the EGOLD+ (Analog Interface B1, C1) via audio amplifier inside the ASIC (D361). Input EPN1_FIL - EPP1_FIL. Output for external loudspeaker AUDIO_L - AUDIO_R, for internal Loudspeaker EPP! – EPN1. The ringing tones are generated with the loudspeaker too. To activate the ringer, the signal RINGIN from the EGOLD+ (Miscellaneous,D16) is used



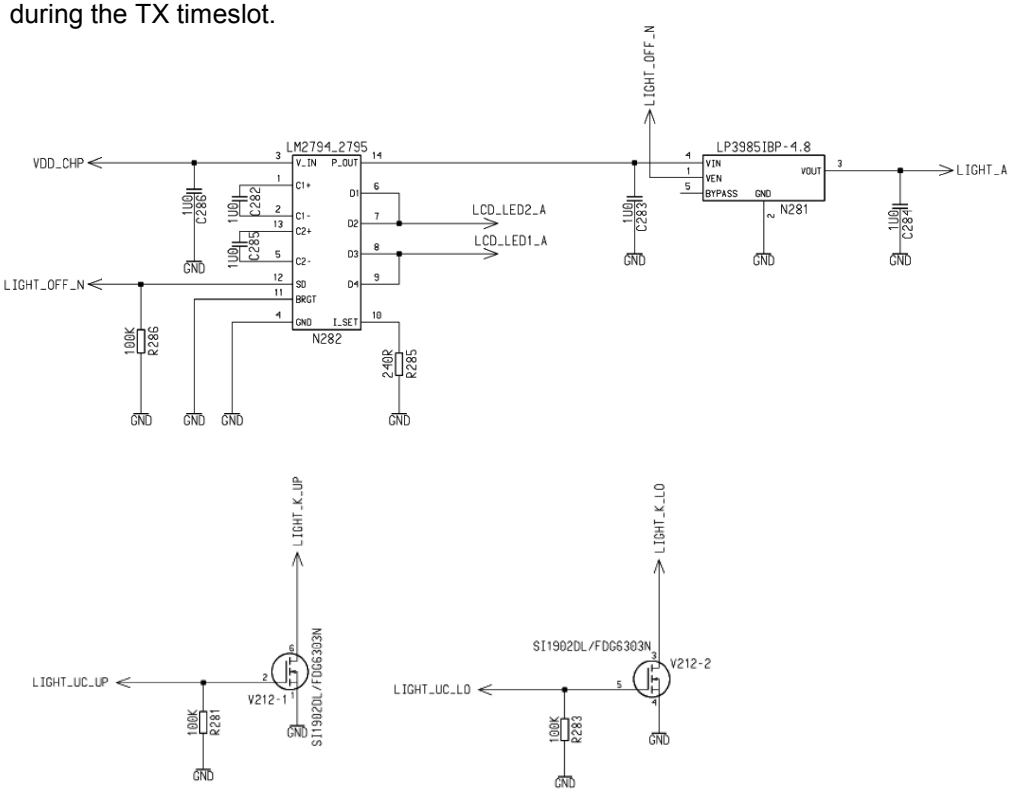
9 Display and Illumination

9.1 Display

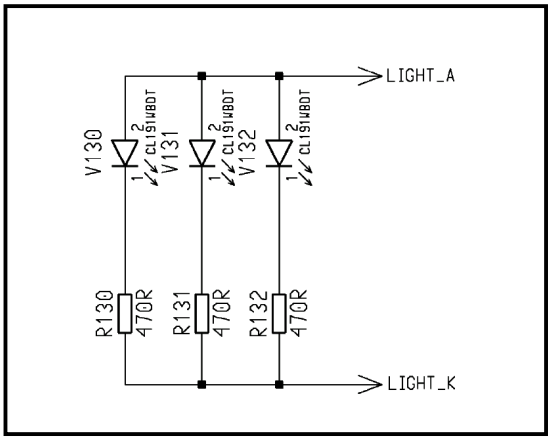
The display is provided with 2,9V from the ASIC (D361). The communication with the EGOLD+ by the LCD-Signals, directly connected to the EGOLD+

9.2 Illumination

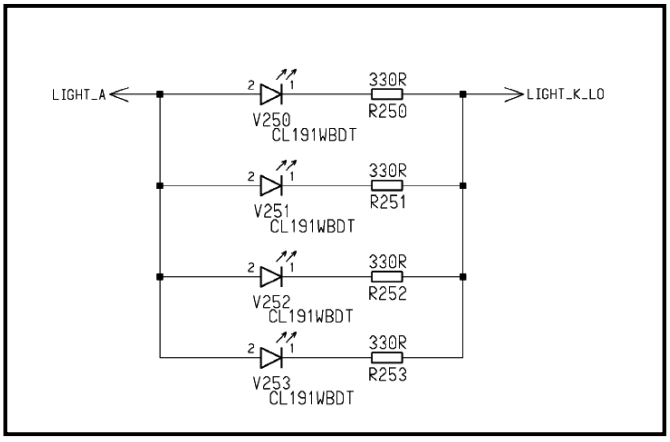
The light is switched via switches inside the EGOLD+. With the signal LIGHT_UC (Miscellaneous T17) the illumination for the keyboard and the display backlight is controlled. With LIGHT_OFF_N. (GSM TDMA-Timer G15) the illumination can be switched “on” and “off” during the TX timeslot.



Display Illumination placed on the MMI Board



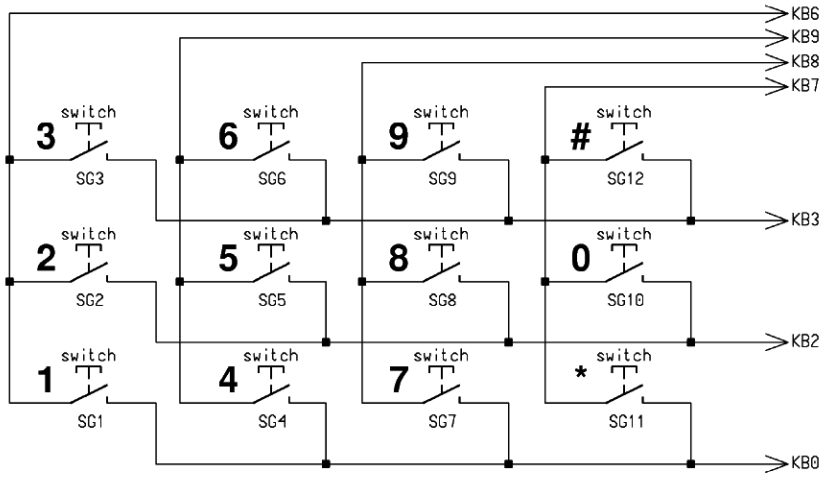
Keypad Illumination placed on the Main Board



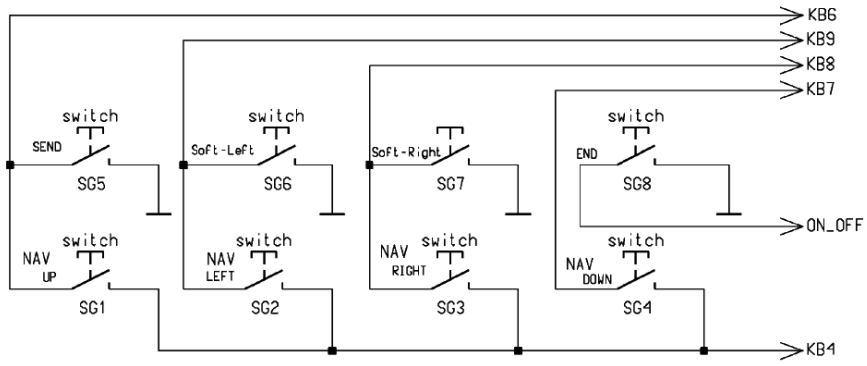
10 Keyboard

The keyboard is connected via the lines KB0 – KB9 with the EGOLD+.
The lines KB0 – KB5 are used as output signals. In the matrix KB6, KB8 and KB9 are used as input signals for the EGOLD+.

Main Keyboard



MMI Keyboard



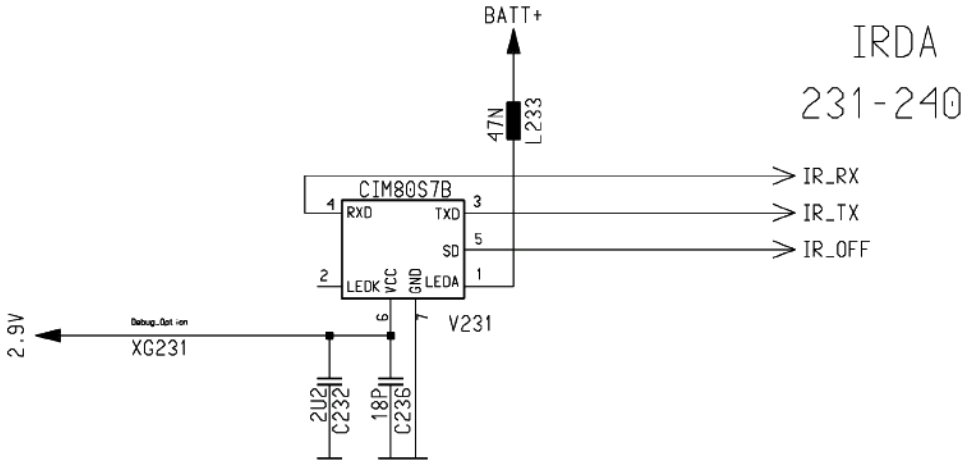
11 IRDA

Low-Power infrared data interface, compatible to ”IRDA - Infrared Data Association; Serial Infrared Physical Layer Specification, Version 1.3”, supporting transmission rates up to 115.2kbps (Slow IRDA). As a Low-Power-Device, the infrared data interface has a transmission range of at least:

- 20cm to other Low-Power-Devices and
- 30cm to Standard-Devices

The viewing angle is +/-15° (resulting in 30° viewing cone).

It is not possible to use the IRDA interface and the Bluetooth interface at the same time.



Name	IN/OUT	Remarks
IR_OFF	IN	Activate IRDA
IR_TX	IN	TX (serial interface multiplexed with Bluetooth)
IR_RX	OUT	RX (serial interface multiplexed with Bluetooth)