Service Manual Level 3
for

BenQ mobile

M81

Release	Date	Department	Notes to change
R 1.0	01.09.2006	ISC S CES	New document

Table of Content

1 Introduction

1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ Mobile repair level 3.

1.2 Scope

This document is the reference document for all BenQ Mobile authorised Service Partners which are released to repair BenQ Siemens mobile phones up to level 3.

1.3 Terms and Abbreviations

2 List of available level 3 parts

(according to Component Matrix V1.18 - check C-market for updates)

Product	ID	Order Number	Description CM
M81	D1000	L50610-G6284-D670	IC SGOLD2PMB8876V2.1
M81	D1250		IC FLASHSDRAM512MB128MBBGA108
M81	D1300	L50645-J4683-Y22	IC ASIC D1094ED-MOZART+TWIGO4+
M81	D1301	L50610-B6189-D670	IC LOGIC 2INPUTNANDNC7SP00L6X
M81	D1302	L50610-B6186-D670	IC LOGIC 2INPUTANDNC7SZ08L6X
M81	D5100	L50610-U6122-D670	IC BLUETOOTHBRF6150PB-FREE
M81	D5400	L50610-L6156-D670	IC AUDIOVIDEOINTERFACEW2182
M81	L1301	L50651-F5103-M1	COIL10U(Co-Type9)
M81	L1302	L36151-F5103-M7	COIL10U(Co-Type2)
M81	L1318	L50640-F2100-Y9	COIL-FILTER0603(Co-Type11)
M81	N1330	L50620-C6258-D670	IC DCDCBOOSTCONVERTERLM2733
M81	N3501	L50610-C6153-D670	IC ANARE2.9VUSMD5PBFREE
M81	N3800	L36145-K280-Y258	IC FEMHITACHIGSM90018001900(Fem-Type1)
M81	N3801	L50651-Z2002-A76	IC MODULPAPF09026B(PA-Type4)PBFree
M81	N3911	L50620-L6159-D670	IC TRANCEIVERHD155153NP
M81	N4800	L50610-C6153-D670	IC ANARE2.9VUSMD5PBFREE
M81	N5400	L50620-C6256-D670	IC ANALM2770
M81	R3967	L36120-F4223-H	RESISTORTEMP22K(Res-Type7)
M81	V1302	L36840-D5076-D670	DIODESOD323(Di-Type7)
M81	V1303	L36840-D5076-D670	DIODESOD323(Di-Type7)
M81	V1305	L36830-C1107-D670	TRANSISTORSI5933(Tra-Type2)
M81	V1400	L50640-D70-D670	DIODEBAV99T(Di-Type9)
M81	V2100	L50640-D5084-D670	DIODERB548W(Di-Type8)
M81	V2302	L36840-C4014-D670	TRANSISTORBC847BSBC846S(Tra-Type7)
M81	V2330	L36840-C4014-D670	TRANSISTORBC847BSBC846S(Tra-Type7)
M81	V3961	L36840-D61-D670	DIODE1SV305(Di-Type4)
M81	V3962	L36840-C2074-D670	IC DACDAC3550A
M81	V4901	L36840-C4014-D670	TRANSISTORBC847BSBC846S(Tra-Type7)
M81	V4902	L50640-L2108-D670	FLASH-LEDHIGHBRIGHTN.WHITE
M81	X1400	L36334-Z97-C213	CONNECTORBATTERY3-POL
M81	X1400	L36334-Z97-C213	CONNECTORBATTERY3-POL
M81	X1504	L50634-Z93-C364	IO-JACKNANO12-POL
M81	X1504	L50634-Z93-C364	IO-JACKNANO12-POL
M81	X1604	L36334-Z97-C337	CONNECTORSIMCARDREADERK1
M81	X1604	L36334-Z97-C337	CONNECTORSIMCARDREADERK1
M81	X2200	L50634-Z97-C380	CONNECTORDISPLAY20POL
M81	X2200	L50634-Z97-C380	CONNECTORDISPLAY20POL
M81	X2705	L50634-Z97-C363	CONNECTORBOARDTOBOARD14-POL.X75
M81	X2705	L50634-Z97-C363	CONNECTORBOARDTOBOARD14-POL.X75
M81	X3500	L50634-Z97-C516	CONNECTORHYDRA-CAMERA-SOCKET
M81	X3500	L50634-Z97-C516	CONNECTORHYDRA-CAMERA-SOCKET

M81	X3800	L36334-Z93-C297	CONNECTORANTENNA6mm
M81	X3800	L36334-Z93-C297	CONNECTORANTENNA6mm
M81	X4800	L50634-Z97-C348	CONNECTORRS-MMC-READERX75
M81	X4800	L50634-Z97-C348	CONNECTORRS-MMC-READERX75
M81	Z1001	L50645-F102-Y40	QUARZ32,768KHZ(Q-Type4)
M81	Z1501	L50620-U6067-D670	FILTEREMI(Fi-Type8)PBFree
M81	Z1601	L50620-U6029-D670	FILTEREMI(Fi-Type6)PBFree
M81	Z1601	L50620-U6029-D670	FILTEREMI(Fi-Type6)PBFree
M81	Z3961	L36145-F260-Y17	QUARZ26MHZ(Q-Type1)
M81	Z5100	L50645-K280-Y330	FILTERBPBLUETOOTH

3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** ***Nano*** Lumberg connector (F30032-P77-A3)
- Troubleshooting Frame S75 (F30032-P492-A1)
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

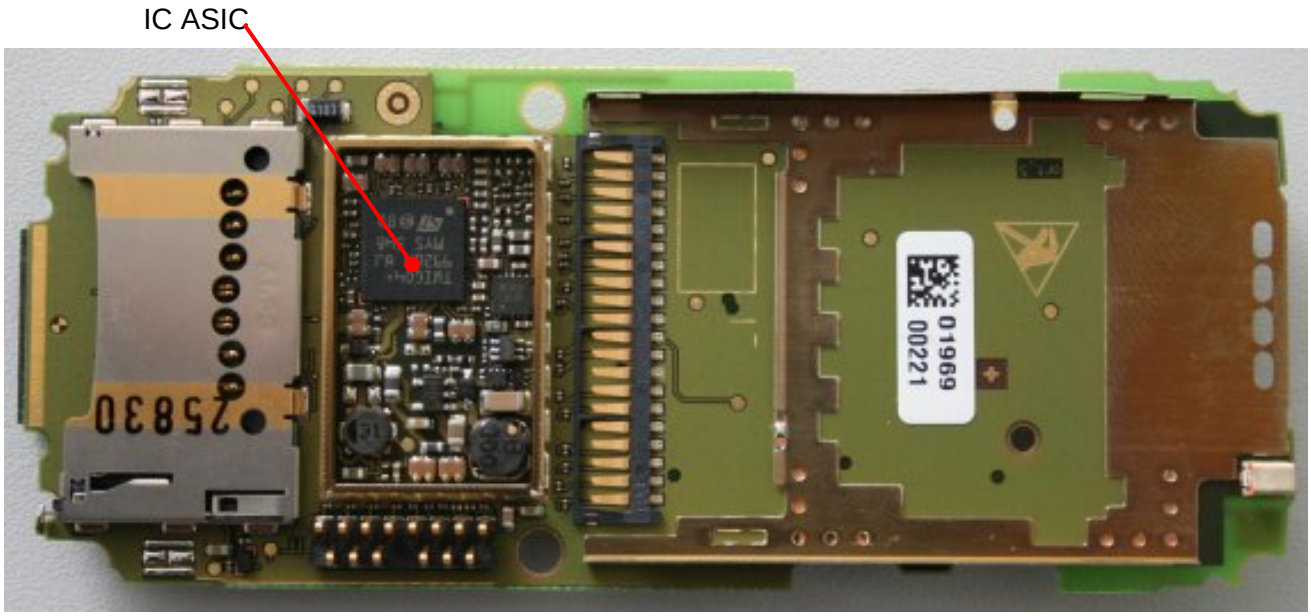
Reference: Equipment recommendation V1.6
(downloadable from the technical support page)

4 Required Software for Level 3

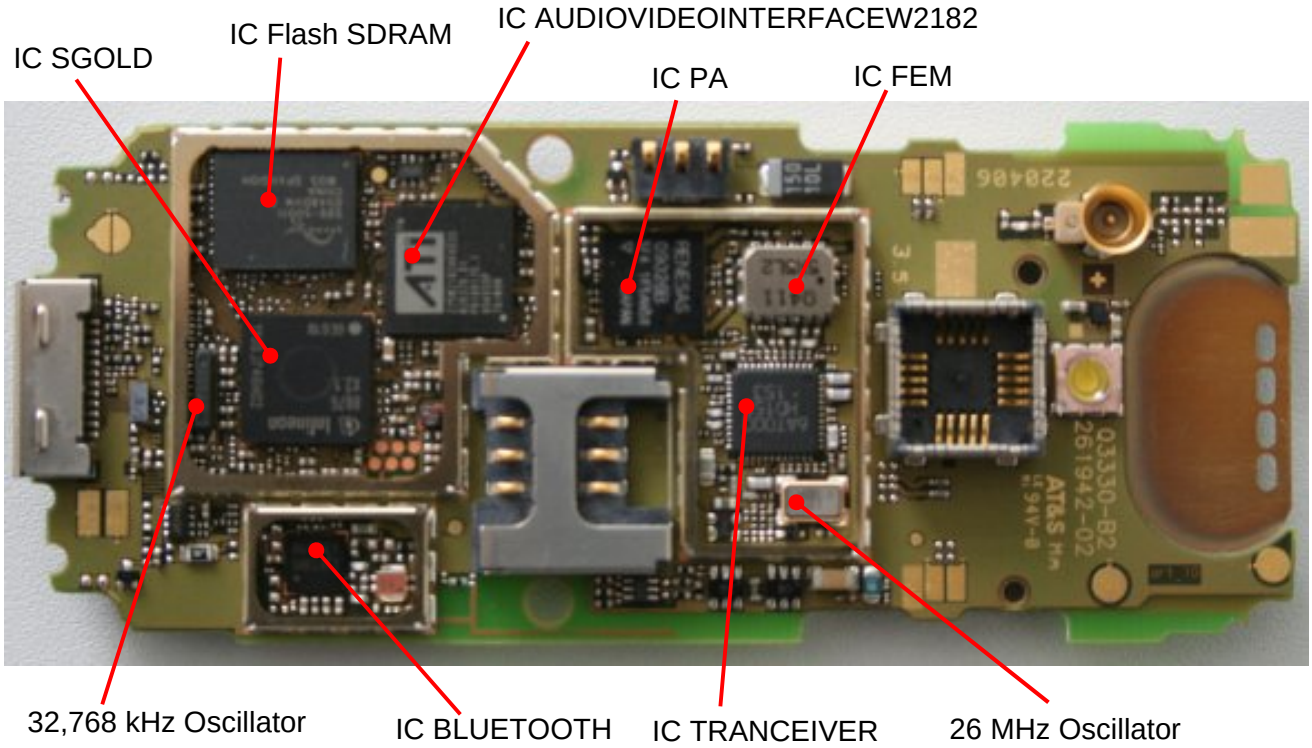
- Windows XP
- X-Focus version 2.20 or higher
- GRT Version 4.03 or higher
- Internet unblocking solution (JPICS)

5 PCB Main Board Overview

PCB Main Board Top Side



PCB Main Board Back Side



6 Radio Part

The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

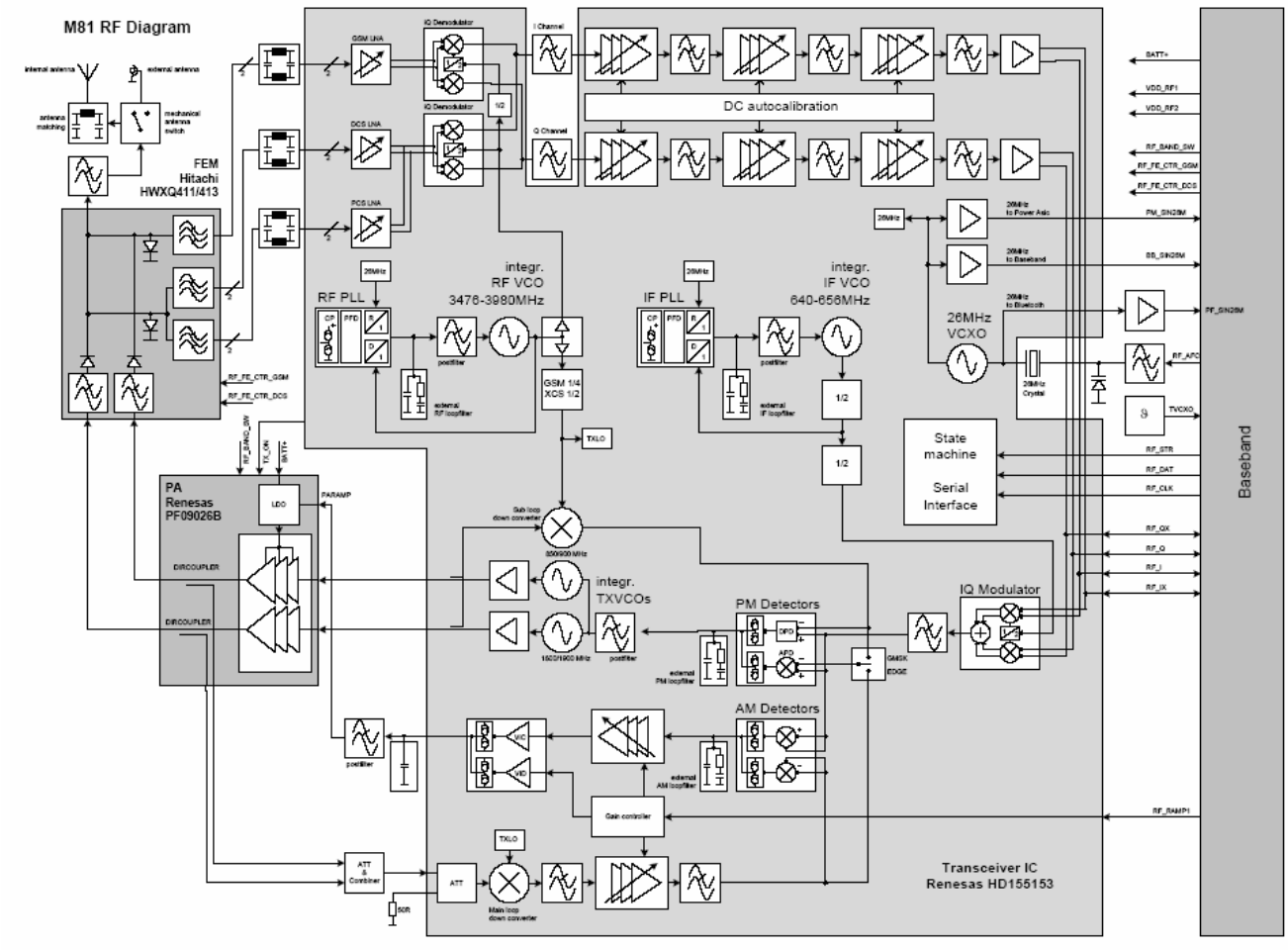
Transmitter and Receiver are never active at the same time. Simultaneous receiving in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible. Simultaneous transmission in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

M81 RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000) supporting GPRS functionality up to multiclass 10.

The RF-circuit consists of the following components:

- Renesas Bright 5PL chip set (HD155153NP) with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2 (without loop filter)
  - Integrated TxVCO (without loop filter and core inductors for GSM)
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - Active part of 26 MHz reference oscillator
  - Integrated Polar Loop, phase and amplitude control of transmitted output power
- Renesas LTCC transmit PA PF09026B (incl. integrated power control circuitry for GMSK mode)
- Frontend-Module including RX-/TX-switch and EGSM900 / DCS1800 / PCS 1900 receiver SAW-filters
- Crystal and passive circuitry of the 26MHz VCXO reference oscillator

6.1 Block diagram RF part

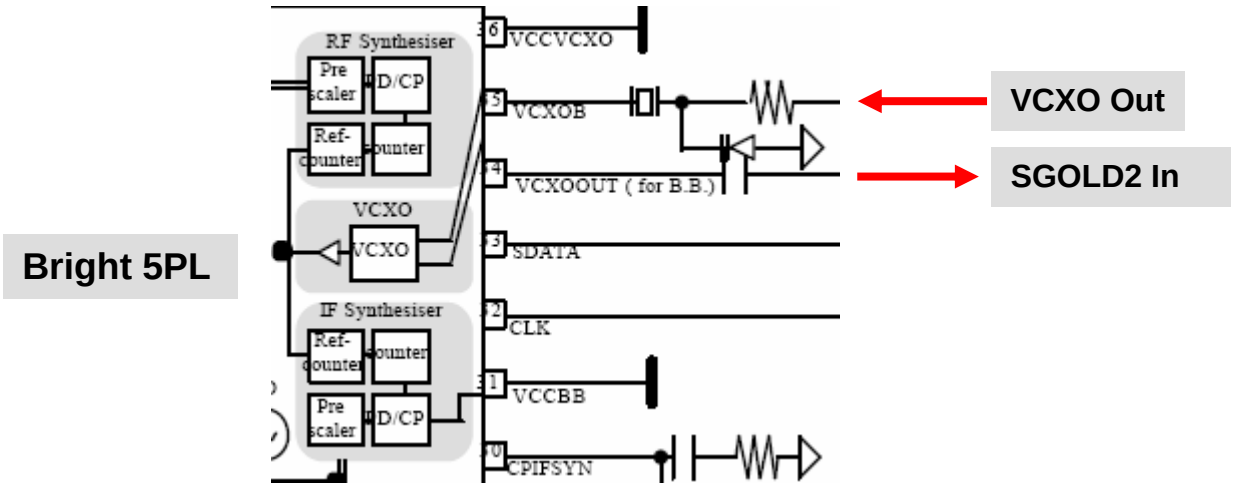


6.2 Power Supply RF-Part

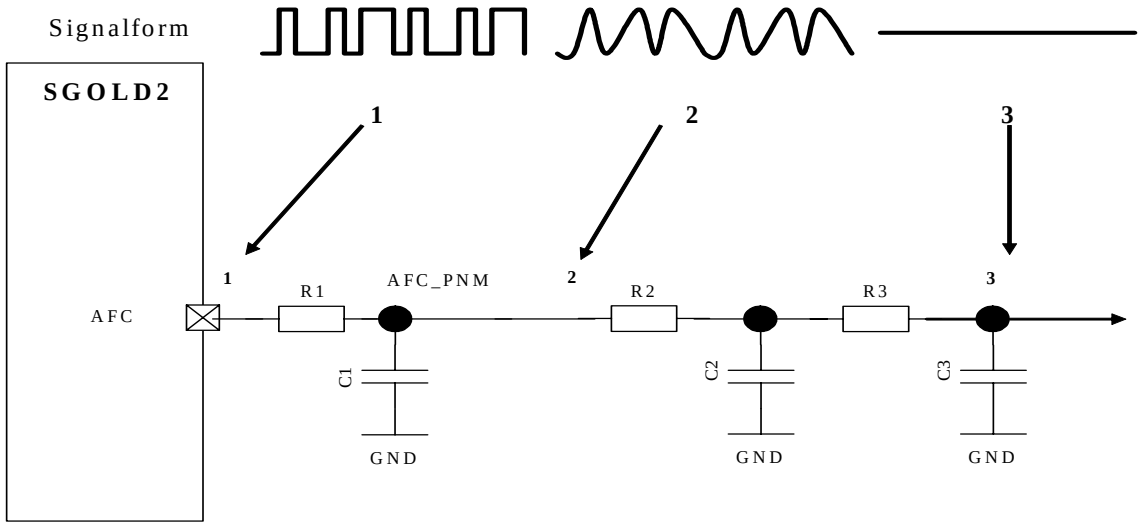
The voltage regulator for the RF-part is located inside the ASIC D1300. It generates the required 2,8V “RF-Voltages” named VDD_RF1 and VDD_RF2. VDD_RF2. The voltage regulator is activated as well as deactivated via VCXOEN_UC (Functional K19) provided by the SGOLD2. The temporary deactivation is used to extend the stand by time.

6.3 Frequency generation

The 26 MHz signal is created by a discrete VCXO (Z3961). The active part is realised within the Bright. For temperature measurements of the VCXO a temperature sensor (R3967) is used. The frequency of the reference oscillator can be fine tuned by the SGOLD2 via a filtered PNM modulated AFC signal (RF_AFC). Two active buffer stages are included in Bright 5PL to provide clock signals for the SGOLD2 and the Power Supply ASIC (BB_SIN26M). An additional external buffer (V3962) is used to deliver a 26MHz clock signal to the Bluetooth chip (BT_SIN26M).



The required voltage VDD_RF1 is provided by the ASIC D1300



Waveform of the AFC signal from SGOLD2 to Oscillator

Synthesizer: LO1

First local oscillator (LO1) consists of a PLL and VCO inside Bright (N3911) and an external loop filter (C3901, C3902).

RF PLL
The minimum frequency step is 400 kHz in GSM1800/GSM1900 mode and 800kHz in EGSM900 bands due to the internal divider by two for GSM1800/GSM1900 and divider by four for EGSM900. The PLL is controlled by the internal state machine which is connected to the SGOLD2 via tree-wire-bus.(RF_DAT; RF_CLK; RF_STR)

RFVCO (LO1)
The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The full oscillation range is divided into 16 sub bands and covers 3476 to 3980MHz. To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the SGOLD2, according to the network channel requirements.

Synthesizer: LO2

The second local oscillator (LO2) consists of a PLL and a VCO which are integrated in Bright 5PL (N3911)and a second order loopfilter which is realized external (C3940, C3941, R3952). Due to the direct conversion receiver architecture, the LO2 is only required for transmit operation in order to generate the transmit IF. To avoid inband spurious in the transmit signal the TX IF frequency is not fixed for the whole band. The LO2 covers a frequency range from 640 to 656MHz.
Before the LO2 signal enters the modulator it is divided by 8. So the resulting TX IF frequencies are 80/82 MHz. The complete LO2 operation is controlled by the Bright internal state machine.
he LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (SGOLD2 signals RF_DAT; RF_CLK; RF_STR). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2nd PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

The required voltage VDD_RF1 is provided by the ASIC D1300

Frontend-Module (FEM)

The frontend module (N3800) includes the RX/TX- and band-switch function based on a combined PIN diode and diplexer-circuit. In the transmit paths a harmonic filtering for EGSM900 and GSM1800/GSM1900 is realized to avoid additional discrete filters. The isolation in TX OFF mode is used to achieve the isolation which is necessary before the active part of the burst. Two lines from the SGOLD2 control the band-selection of the TX switches (RF_FE_CTRL_GSM, RF_FE_CTRL_GSM). The three receiver chains include SAW filter for EGSM900, GSM1800 and GSM1900 to protect the receivers from strong blocking signals.

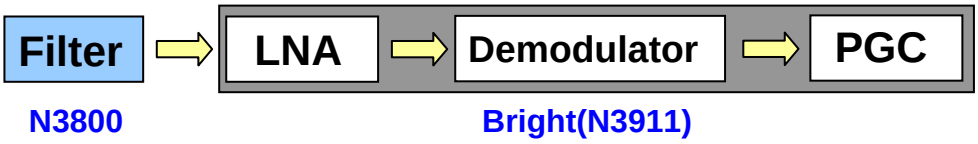
6.4 Receiver

Receiver: Filter to Demodulator

The Bright 5PL incorporates three RF LNAs for EGSM900, GSM1800 and GSM1900 operation followed by direct conversion mixers which are IQ demodulators. The LNA/mixer can be switched in normal-, low- and lower-gain mode. For the “normal gain“ state the mixers are optimised in terms of conversion gain and noise figure, in the “low gain“ state the mixers are optimised for large-signal behaviour for operation at a high input power levels. The "lower gain mode" reduces the RF-level by activating a differential impedance in front of the LNA to improve the large signal performance.

Furthermore the IC includes a programmable gain baseband amplifier PGA (90dB control range, 2dB steps) with automatic DC offset calibration. The channel filtering is realized inside the chip with a four stage baseband filter for both IQ chains. Only two capacitors which are part of the first passive RC-filters are external (C3905, C3906). The second, third and fourth filters are active filters and are fully integrated. The distributed channel filter is necessary to suppress adjacent channel and inband-blocking interferer to avoid any compression in each amplifier stage.

The downconverted IQ signals are fed into the A/D converters inside the SGOLD2. By a special algorithm the level of the IQ signals is kept constant on a defined level by varying the PGA gain and selecting the appropriate LNA gains.

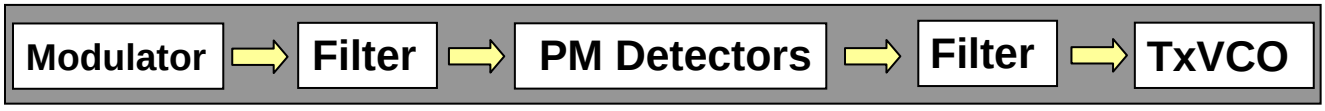


The required voltage VDD_RF1 and VDD_RF2 are provided by the ASIC D1300

6.5 Transmitter

Modulator

The generation of the modulated RF signal in Bright 5PL (N3911) is based on the principle of the polar loop architecture. The IQ signals generated by the SGOLD2 baseband are modulated to the transmit IF of 80MHz by an IQ modulator. The required carrier frequency is provided by the LO2.
As in an conventional upconversion loop the IF signal is up-converted to the transmit frequency. Therefore a down-converter and a phase detector are used in order to compare the IF signal to the down-converted transmit signal. This loop is called PM loop and is used for GMSK operation.
In 8PSK mode the 80MHz IF signal is split into PM and AM components. A second loop is then used to control the AM components. Therefore an AM detector is implemented which compares the 80MHz IF signal and the down-converted transmit signal. The AM loop is also used for power ramping. Inside the AM loop there are two analogue gain controlled amplifiers. These are used for setting the output power level and to keep the loop bandwidth constant.
The separated AM and PM components of an 8PSK signal are finally fit together inside the PA. The PA is driven by the TXVCO signals containing the PM components. The AM component is added by an amplitude control input pin, which controls the supply voltage of the RF transistors and therefore the PA output power level.



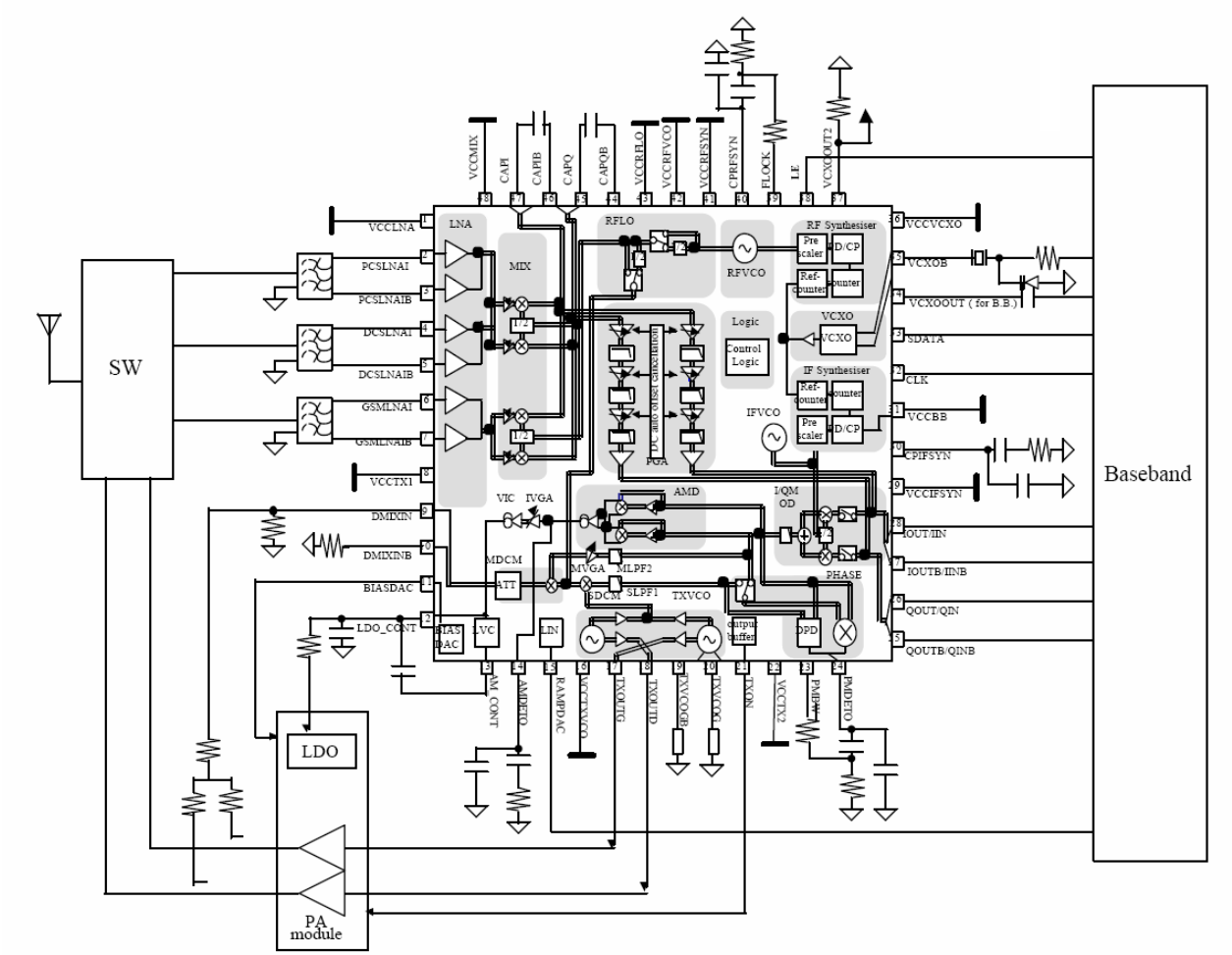
Bright(N3911)

The required voltage VDD_BRIGHT is provided by the ASIC D1300

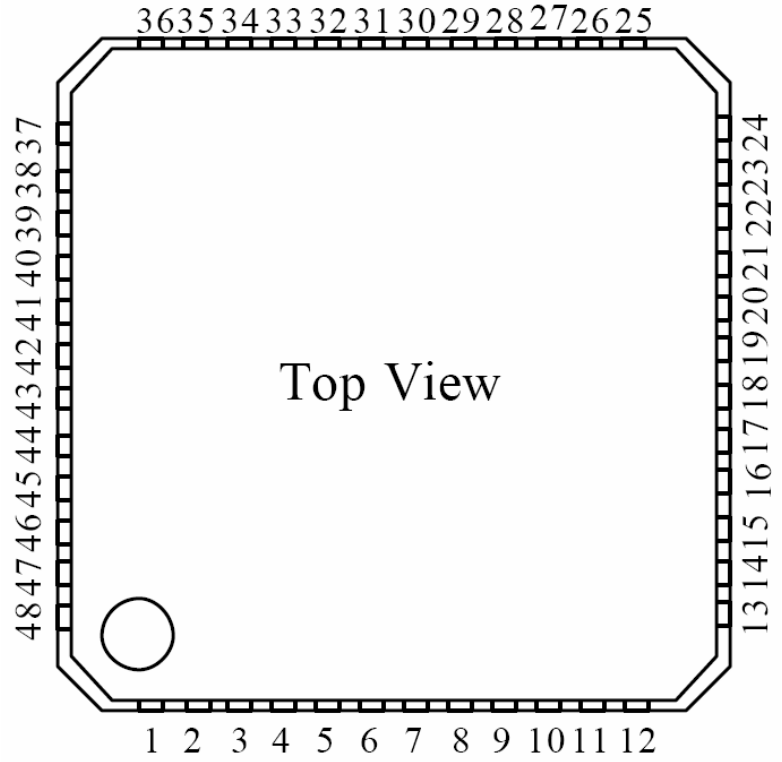
6.6 Bright IC Overview

BRIGHT 5PL

IC Overview

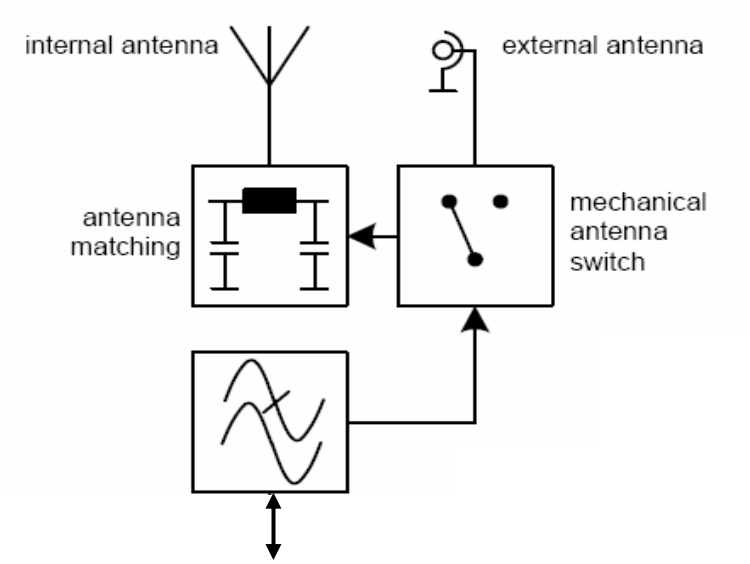


IC top view



6.7 Mechanical Antenna switch

The M81 mechanical antenna switch, for the differentiation between the internal and external antenna.



6.8 Power Amplifier and Power Control

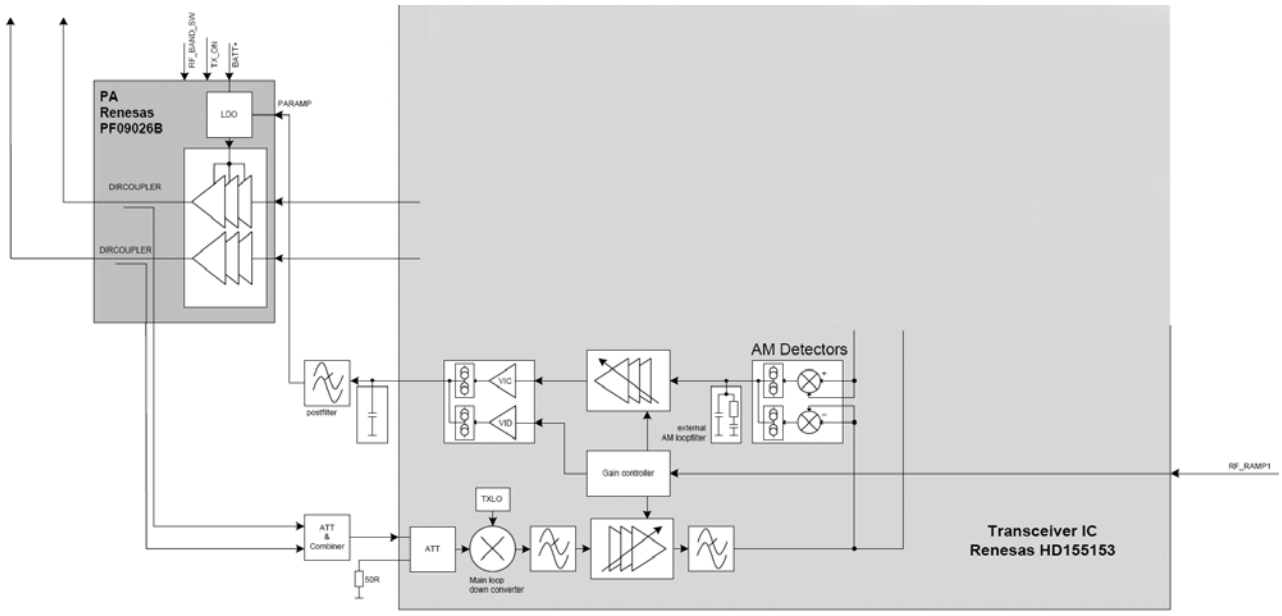
PA

The power amplifier is a LTCC (Aluminia-oxyd-ceramic) PA module, matched to 50 Ω at all signal ports. It contains two separate 3-stage amplifier chains for EGSM900 and GSM1800/GSM1900 operation. It is possible to control the output power level of both bands via one VRAMP port. The appropriate amplifier chain is activated by a logic signal, which is provided by the SGOLD2 (RF_BAND_SW). The module is switched on by a control signal generated by the Bright5PL internal state machine (TX_ON). The RF transistor bias voltage is generated inside the PA module. The PA module consist also of two additional directional coupler to provide the needed RF feedback signal for the AM control in 8PSK Mode.

The required voltage BATT+ is provided by the battery.

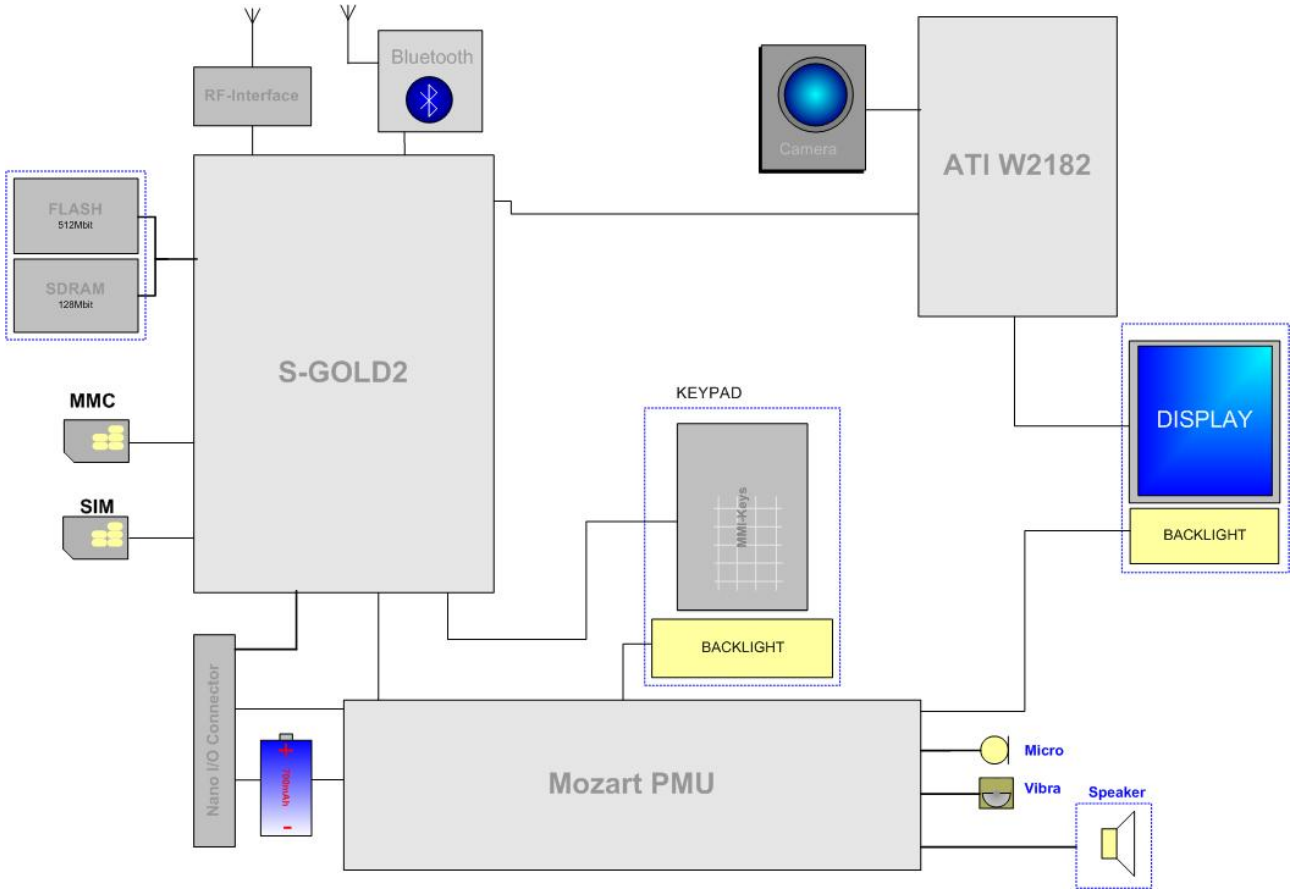
Power Control

In GMSK operation the output power is directly controlled by a control voltage coming from SGOLD2. This voltage is fed through Bright5PL and connected to the PA module (PARAMP).
In 8PSK operation the AM loop controls the output power level. Therefore the same SGOLD2 signal is used but connected to the variable gain amplifiers inside Bright5PL. The AM control voltage finally controls the PA module (PARAMP). All switching between GMSK and 8PSK modes is controlled by the Bright5PL internal state machine.



7 Logic / Control

7.1 Overview Hardware Structure M81



7.2 SGOLD2

Baseband Processor SGOLD2 Features

Supported Standards

• EGPRS class 12 MCS 1..9
• GSM speech FR, HR, EFR and AMR-NB
• GSM data 2.4kbit/s, 4.8kbit/s, 9.6kbits, and 14.4kbit/s
• HSCSD class 10
• GPRS class 12 CS 1..4

Processing cores

• ARM926EJ-S 32 bit processor core with operating frequency up to 156 MHz for controller functions. The ARM926EJ-S includes an MMU, and the Jazelle Java extension for Java acceleration.
• TEAKLite® DSP core with operating frequency 138.67 MHz.

ARM-Memory

TEAKLite®-Memory (word: 16bit)

Shared Memory Blocks (word: 16bit)

Controller Bus System

TEAKLite® Bus System

Clock System

The clock system allows widely independent selection of frequencies for the essential parts of the S-GOLDliteTM. Thus power consumption and performance can be optimized for each application.

Functional Hardware blocks

• CPU and DSP Timers
• Programmable PLL with additional phase shifters for system clock generation
• GSM Timer Module that off-loads the CPU from radio channel timing
• GMSK Modulator according to GSM-standard 05.04 (5/2000)
– GMSK Modulator: gauss-filter with B*T=0.3
• Hardware accelerators for equalizer and channel decoding
• A5/1, A5/2, A5/3 Cipher Unit
(A5/3 added in S-GOLDliteTM V1.1)
• GEA1, GEA2, GEA3 Cipher Unit to support GPRS data transmission
(GEA3 added in S-GOLDliteTM V1.1)
• Advanced static and dynamic power management features including TDMA-Frame synchronous low-power mode and enhanced CPU modes (idle and sleep modes)
• Incremental Redundancy Memory for EDGE class 12 support
• GMSK / 8-PSK Modulator according to GSM-standard 05.04 (5/2000)
– GMSK Modulator: gauss-filter with B*T=0.3
– EDGE Modulator: 8PSK-modulation with linearised GMSK-pulse-filter
• MOVE coprocessor performing motion estimation for video encoding algorithms
(H.263, MPEG-4)

Signal Processing Firmware Support

- FR, HR, EFR, and AMR
- data transmission channel codecs for 2.4, 4.8, 9.6 and 14.4 kbit/s
- HSCDS class 10 support
- GPRS class 12 support with coding schemes CS1..4
- Support for Handsfree, side- and signaling tone generation
- MMS-support
- EGPRS class 12 with modulation and coding schemes MCS1..9 (Release 5 compliant)
- Polyphonic ringer for up to 64 voices at sampling rates up to 48kHz
- 64 voices midi (pseudo) stereo
- enhanced audio visualization
- voice control

Interfaces and Features

- Keypad Interface for scanning keypads up to 8 rows and 8 columns
- Pulse Number Modulation output for Automatic Frequency Correction (AFC)
- Serial RF Control Interface; support of direct conversion RF
- 2 USARTs
- IrDA Controller
- 1 Serial Synchronous SPI compatible interfaces in the controller domain
- 1 Serial Synchronous SPI compatible interface in the TEAKLite® domain
- I2C-bus interface
- 2 bidirectional and one unidirectional I2S interface accessible from the TEAKLite®
- USB V1.1 mini host interface
- IEEE 1149.1 compliant JTAG port for Boundary Scan and debug
- ISO 7816 compatible SIM card interface
- Enhanced digital (phase linearity, adj/ co-channel interference) baseband filters, including analog prefilters and high resolution analog-to-digital converters.
- Digital and analog audio filters including wideband audio capable digital-to-analog and analog-to-digital converters.
- Audio front-end will be accessible from MCU (via shared memory) and the TEAKLite® (i.e. voice recognition and echo cancellation can run on TEAKLite®)
- Hifi Stereo voiceband with CD-Quality
- Separate analog-to-digital converter for various general purpose measurements like battery voltage, battery, VCXO and environmental temperature, battery technology, transmission power, offset, onchip temperature, etc.
- Ringer support for highly oversampled PDM/PWM input signals for more versatility in ringer tone generation
- Differential VMIC generation
- RF power ramping functions
- DAI Interface according to GSM 11.10 is implemented via dedicated I2S mode
- 26 MHz master clock input
- External memory interface:
- Port logic for external port signals
- Comprehensive static and dynamic Power Management

– Various frequency options during operation mode
– 32 kHz clock in standby mode
– Sleep control in standby mode
– RAMs and ROMs in power save mode during standby mode

- Debug Features

- 2 General Purpose Timers with 3 32-bit timers
- Serial number
- A real time clock with alarm functions
- 2 capture/compare units with 16 channels
- A fast parallel Display Interface
- Camera Interface
- Programmable clock output for a camera
- An Multimedia/Secure Digital Card Interface (MMCI/SD; SDIO capable)
- A Flash Controller DMA Port (FCDP) supporting NAND flash
- A multimedia extension interface (MMIC-IF) supporting external hardware accelerator
- A Fast IrDA Interface
- A Universal Serial Interface (USIF) enabling asynchronous or synchronous serial data transmission.

7.3 SDRAM

The SDRAM (Synchronic Dynamic Random Access Memory) is for volatile data.

Memory Size:	128 Mbit (16 MByte)
Data Bus:	16Bit
IO / Core Voltage Supply:	typ. 1.8 V

7.4 FLASH

Code Flash

It is a non-volatile-, re-programmable- memory (SW-updateable), with a high performance interface. The mobile-SW can be executed directly. The Flash has an unchangeable serial number.

Memory Size:	256 Mbit (32 MByte)
Data Bus:	16 Bit
IO / Core Voltage Supply:	typ. 1.8V

Data Flash

Non-volatile re-programmable- memory for saving user data (pictures, sounds, videos etc.)

Memory Size:	256 Mbit (32 MByte)
Data Bus:	16 Bit
IO / Core Voltage Supply:	typ. 1.8V

7.5 SIM

SIM cards with supply voltages of 1.8V and 3V are supported..

7.6 Vibration Motor

The vibration motor is mounted in the lower case of the base part. The electrical connection to the PCB is realised with pressure contacts.

8 Display

In the M81 a display module with an intelligent graphic Liquid Crystal Display (LCD) is used. The display module consists of the following parts and features

- an Active Matrix Liquid Crystal Display Panel, 132x176 dots, 262k colours, positive mode
- a display controller mounted on the display glass which is connected to a FPC inside the module
- a light guide with 4 white LED's
- Illumination foil stack is implemented in the module
- A PCB/FPC with all passive components.
- An electrical interface that consists of land pattern designed for spring connector. The 20-pin spring connector is mounted on the PCB
- Parallel 8-bit interface

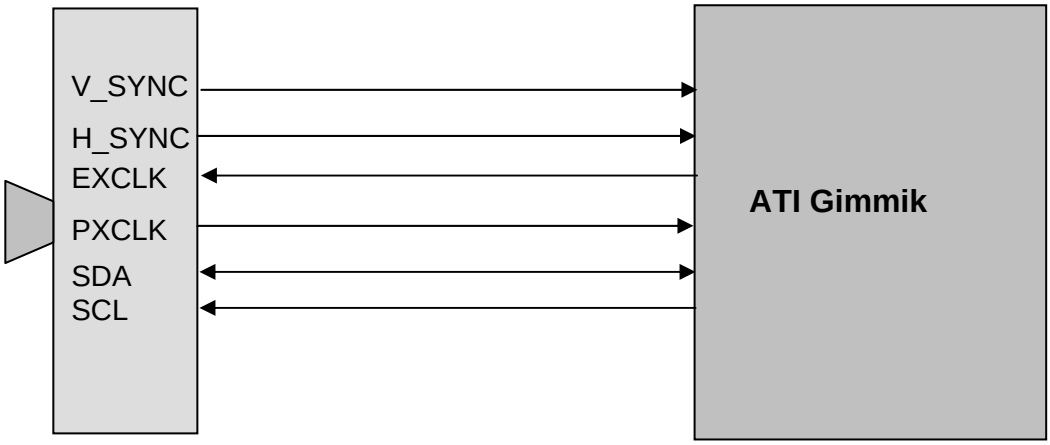
9 ATI Gimmick

The ATI Gimmick W2182 is used as Audio Video Interface.
Gimmick Chip ATI W2182 Features:
JPEG Full Encoder and Decode Acceleration
MPEG-4 Decoder
Advanced 2D Graphics
Video Capture
Audio Support

10 Camera

The camera module consists of a 1.3MPix-CMOS sensor, image processor circuitry, lens and holder, lens hood, cover glass and housing to attach the camera on the PCB. Connectivity from camera module to PCB is realized by using a socket.

Block-diagram



11 Bluetooth

The Bluetooth Interface BRF6150 is compatible to the Bluetooth specification version 1.2 power class 2 (-6 dBm up to +4dBm) with a RX sensitivity better than –70 dBm and support multipoint connections.
It supports a transmission rate up to 723 kBit/s data asymmetrically over the air interface.
The transmission range is approx. 10 m. Between SGOLD2 and BRF6150 a data rate up to 4921.6 8 kbit/s is used.
The following table shows the interface between SGOLD2, ASIC and the BRF6150

Pin name		Signal name	Meaning	Connected to
VDD_IN_BB VDD_IN_RFIO VDD_IN_ANA VDD_IN_OSC	IN	VDD_BT VDD_BT_RF2	Main power supply	ASIC "VREF3"
VDD_IO_x VDD_IO_SF_x	IN	2.65V 2.65V (2.9V)	IO Power supply 2.9V needed for stacked flash	ASIC VDD IO SGOLD REG3 2.65V (REG1 2.9V)
HCI_RTS	OUT	BT_CTS	USART IF	SGOLD2 “USART1_CTS”
HCI_RX	IN	BT_TX	USART IF	SGOLD2 “USART1_TX” or SGOLD2 "USIF_TXD_MSTR"
HCI_TX	OUT	BT_RX	USART IF	SGOLD2 “USART1_RX”or SGOLD2 "USIF_TXD_MSTR"
HCI_CTS	IN	BT_RTS	USART IF	SGOLD2 “USART1_RTS”
AUD_CLK	IN	BT_PCM_CLK	PCM IF	SGOLD2 “I2S1_CLK”
AUD_FSYNC	IN	BT_PCM_SYNC	PCM IF	SGOLD2 “I2S1_WA0”
AUD_IN	IN	BT_PCM_IN	PCM IF	SGOLD2 ”I2S1_TX”
AUD_OUT	OUT	BT_PCM_OUT	PCM IF	SGOLD2 “I2S1_RX”
HCI_TX	OUT	BT_WAKEUP_GM	Wakeup-line, needed if H5 is not used	SGOLD2 “KP_IN6"
NSHUT_DOWN	IN	BT_RESET	Reset	ASIC “Outport”
CLK32	IN	CLK32	32,768 kHz +-250ppm Rectangular wave	S-GOLD2 “CLK32”
XTALP_FAST_CK_IN	IN	BT_SIN26M	26MHz clock signal sine wave	RF-GSM
IO0_EXT_CLK_REQ_OUT	OUT	BT_VCXOEN	26MHz clock request	ASIC “SLEEP2N”

12 Flashlight

The LED Flash Module is controlled by the Gimmick Chip (D5400) and could be operated in two modes. One is the video/ torch mode (low current) and the other the flash mode (high current). The duration of the flash could also be set by the D5400. The Gimmick Chip guarantees that the flash LED is switched off after the defined flash duration especially after a software breakdown.
The flash LED consists of four diodes, which are connected in series. Each diode is driven with about 65mA in flash mode(Pulse) and 7-10mA in the torch mode (DC). The Flash LED would be turned on at least for 2 V-SYNC cycles to guarantee a complete image exposure. The flash LED is only be used in the low light mode of the camera (7,5 fps), that means the minimum switch on time in the flash mode is 266ms. To avoid any damage of the LED the turn on time should not exceed 400ms for high peak currents (~ 70mA).

13 Power Supply

13.1 ASIC Mozart / Twigo4

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- 17 Voltage regulators
- 2 internal DC/DC converters (Step-up(not used) and Step-down converter)
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I^2C interface)
- Bandgap reference
- High performance audio quality
- Audio multiplexer for selection of audio input
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I^2S Interface

13.1.1 Battery

As s standard battery a Li-ion battery with the nominal capacity of 630 mAh @ 0.2 CA * and GSM capacity ** of minimal 600 mAh will be provide.

13.1.2 Charging Concept

13.1.2.1 General

The battery is charged in the phone. The hardware and software is designed for LiIon with 4.2V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the “Charge” symbol in the display). During normal use the phone is being charged (restrictions: see below).
Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the PMU hardware can override/interrupt the charging in the case of over voltage of the battery
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. Charging is ongoing as long the temperature is within the range 0°C to 50°C. The maximal charge time will be 2 hours (I_{max}=750mA).

13.1.2.2 Measurement of Battery voltage, Battery Type and Ambient Temperature

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor, the voltage at battery code capacitor and the ambient temperature.

13.1.2.3 Timing of the Battery Voltage Measurement

Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

13.1.2.4 Recognition of the Battery Type

The different batteries will be encoded by different resistors within the battery pack itself.

13.1.2.5 Charging Characteristic of Lithium-Ion Cells

LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is given by the connected charger. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be performed is in the ranges from 0...50°C. Outside this range no charging takes place, the battery only supplies current.

13.1.2.6 Trickle Charging

The ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the ASIC by means of the external FET. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.2V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the ASIC will switch on the phone automatically and normal charging will be initiated by software.

13.1.2.7 Normal Charging (Fast charge)

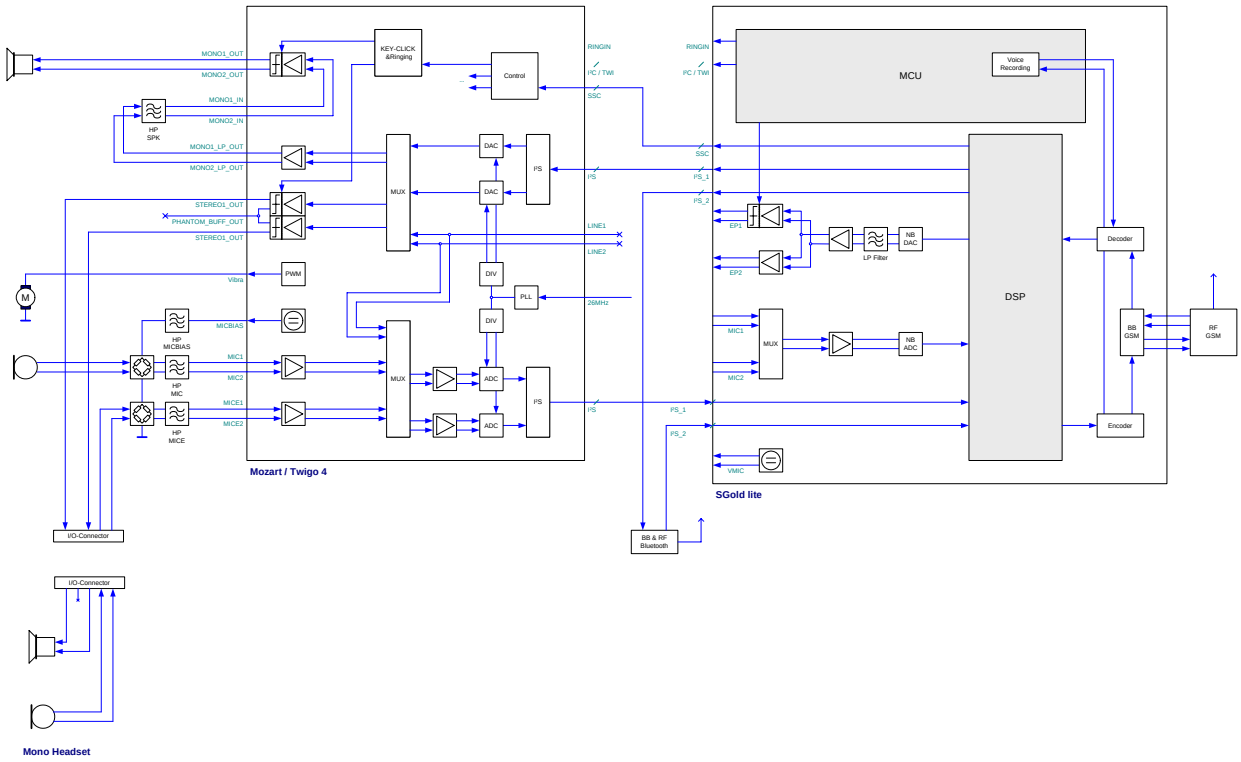
For battery voltages above 3.2 Volt and normal ambient temperature between 0 and 50°C the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the ASIC ASIC. The level of charge current is only limited by the charger.

13.1.2.8 USB Charging

The ASIC can support USB charging when USB charging is integrated in the charging software. If charge voltage is in the range 4.4V to 5.25 V USB charging is ongoing. During USB charging only limited charging is possible. Charge current is limited to 75, 150, 300 or 400 mA.

13.1.2.9 Audio multiplexer

The digital audio information from/to the DSP inside the SGOLD2 are delivered via the I2S interface, the 26MHz from the RF part. The internal AD and DA converter are connected to microphone and loudspeaker.



13.1.2.10 Interface

The ASIC has two serial control interfaces and one serial audio interface. With the serial interfaces, all functions of the ASIC can be controlled. For time critical commands (all audio functions incl. Vibra) the SSC is used.

TWI interface

TWI (two wire interface) is an I2C 2 wire interface with the signals Clock (I2C_CLK) data line (I2C_DAT) and the interrupt (PM_INT).

SSC interface

The SSC interface enables high-speed synchronous data transfer between SGOLD and ASIC.
The interface consist of: clock signal (PM_SSC_SCLK), master transmit slave receive (PM_SSC_MTSR), master receive slave transmit (PM_SSC_MTSR) and the select line (PM_SSC_CS)

IS2 interface

The audio interface is a bidirectional serial interface, TX and RX part are independent. The IS2 interface consist of a three wire connection for each direction. The three lines are clock (CLK), the serial data line (DAC or ADC) and the word select line (WAO). Clock and word select line is used for RX and TX together in SL65. (PM_I2S_DAC for RX and PM_I2S_ADC for TX)

13.1.2.11 LDO`S

LDO´s:	Voltage	Current	Name	voltage domains
REG 1	**2,9V**	0...140mA	2.9V	Display, Epson Camera-Chip, SGOLD2
REG 2a	**1,5V**	0...300mA	1.5V_UC	SGOLD2
REG 2b	**1,5V**	0...100mA	1.5V_DSP	SGOLD
REG 3	**2,65V**	0...140mA	2.65V	SGOLD2, Hall-Sensor, Epson Camera-Chip, USB Switch
MEM REG1	**1,8V**	0...250mA	1.8V_MEM1	SGOLD2, Display, SDRAM
MEM REG2	**1,8V**	0...150mA	1.8V_MEM2	Flash Memory, Camera-ASIC
AUDIO REG	**2,9V**	0...190mA	VAUDREGA	PMU ASIC
RF REG1	**2,7V**	0...150mA	VDD_RF1	RF-Part (Hitachi Bright V)
AFC REG	**2,65V**	0...2mA	VDD_AFC	SGOLD2
LP_REG	**2,0V**	0...2mA	VDD_RTC	SGOLD2
SIM REG	**2,9V**	0...70mA	VDD_SIM	SIM
USB REG	**3,1V**	0...40mA	VDD_USB	SGOLD2, USB Protection
VIBRA	**2,8V**	0...140mA	VDD_VIBRA	VIBRA

13.2 External step-up converter

The stepup converter N1300 supplies the LED for video/torchlight and flash light. It is also used to supply the display and keypad backlight LEDs. The converter is only capable to drive one of the above mentioned modes.

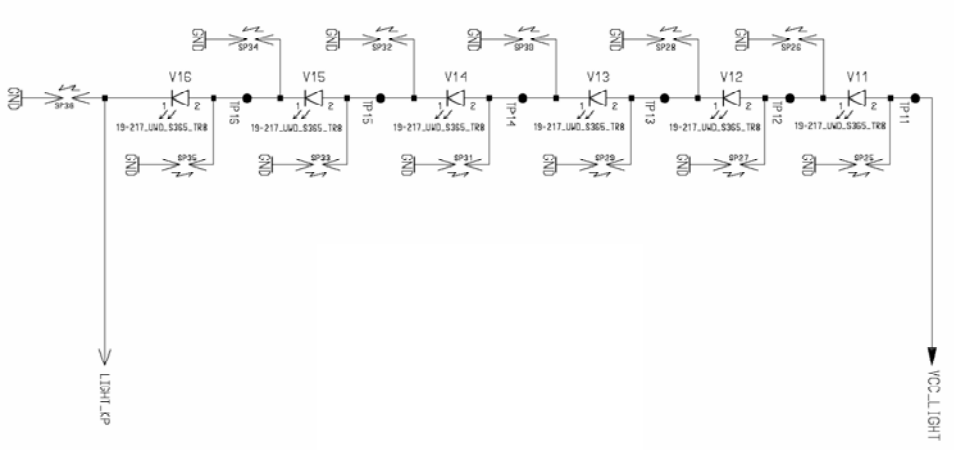
- Video/torchlight supply: V_{OUT} = 19,7V-20,7V; I_{OUT} = 8,3mA
- LED flash supply: 19,7V-20,7V; I_{OUT} = 65mA; 400ms; Duty Cycle 1/10
- Display and Keypad backlight: 19,7V-20,7V; I_{OUT} = 30mA

14 Illumination

a) Keyboard (connected via Board to Board Connector)

LED illuminations of Keypad are controlled by the LIGHT_PWM2 signal. As LEDs are fed from VBOOST/VCC_LIGHT.

The illumination of the keypad will be done via high-brightness LEDs (white color top-shooter, driven by 5mA / LED).

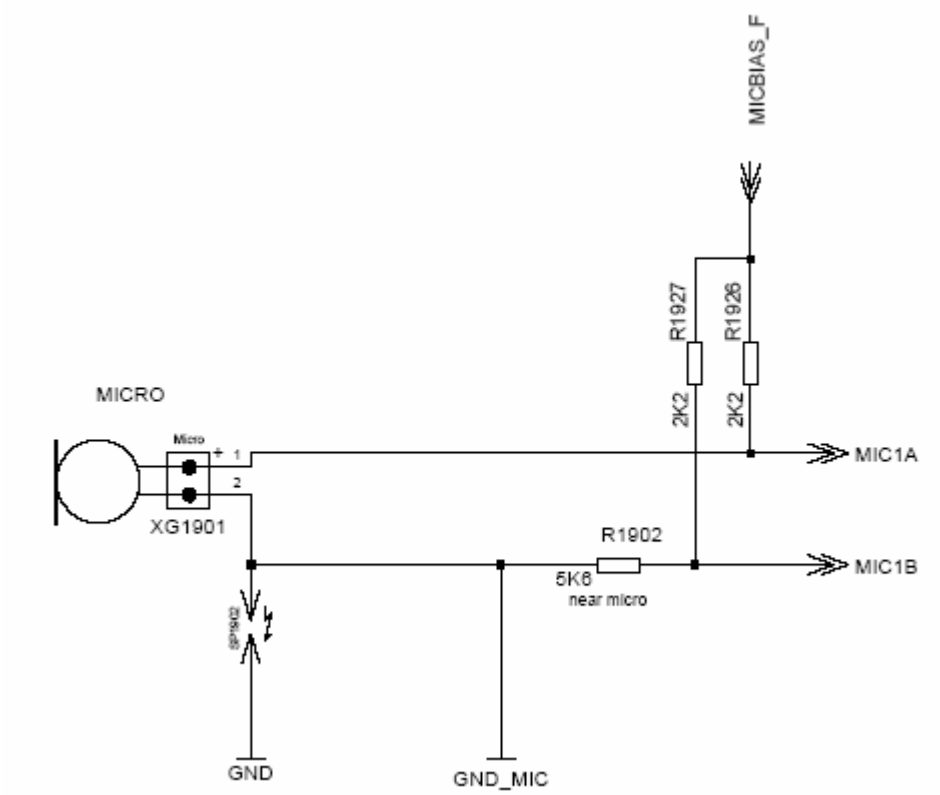


b) Display (connected via Board to Board Connector)

The 4 serial LEDs for the display are supplied by one constant current sources, to ensure the same brightness and color of the white backlight.

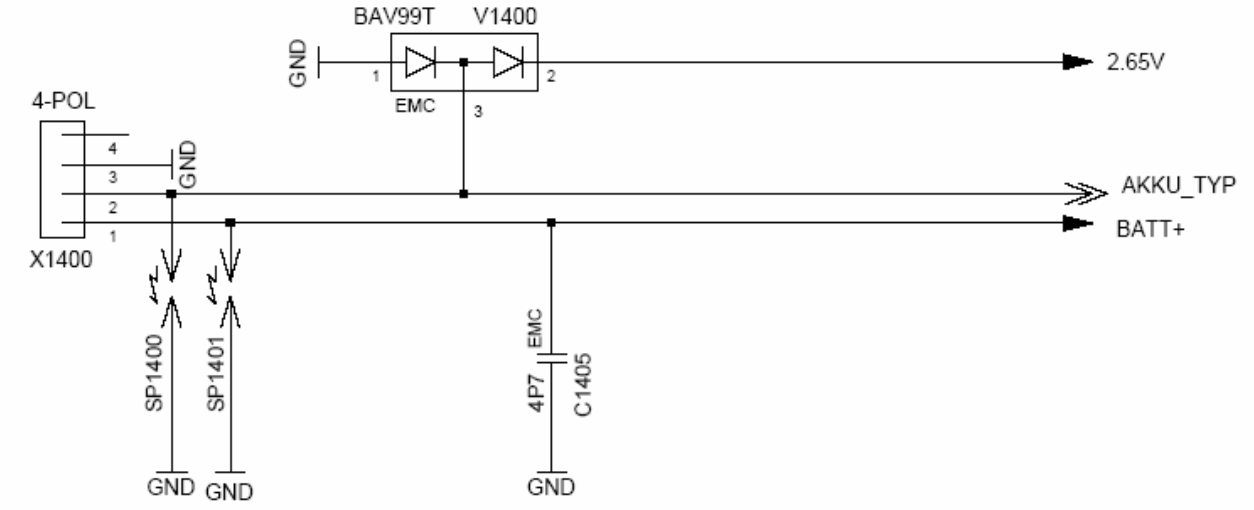
15 Interfaces

15.1 Microphone (XG2001)



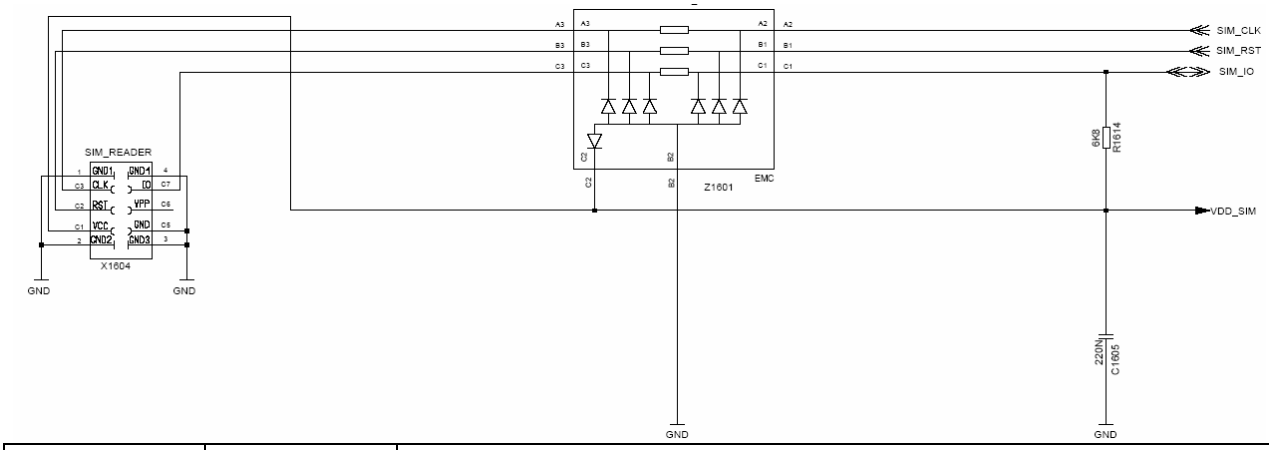
Pin	Name	IN/OUT	Remarks
1	MIC1A	O	Microphone power supply. The same line carries the low frequency speech signal.
2	MIC1B		GND_MIC

15.2 Battery (X1400)



Pin	Name	Remarks
1	BATT+	Positive battery pole
2	AKKU_TYP	Recognition of battery/supplier
3	GND	Ground

15.3 Interface SIM Module with ESD protection

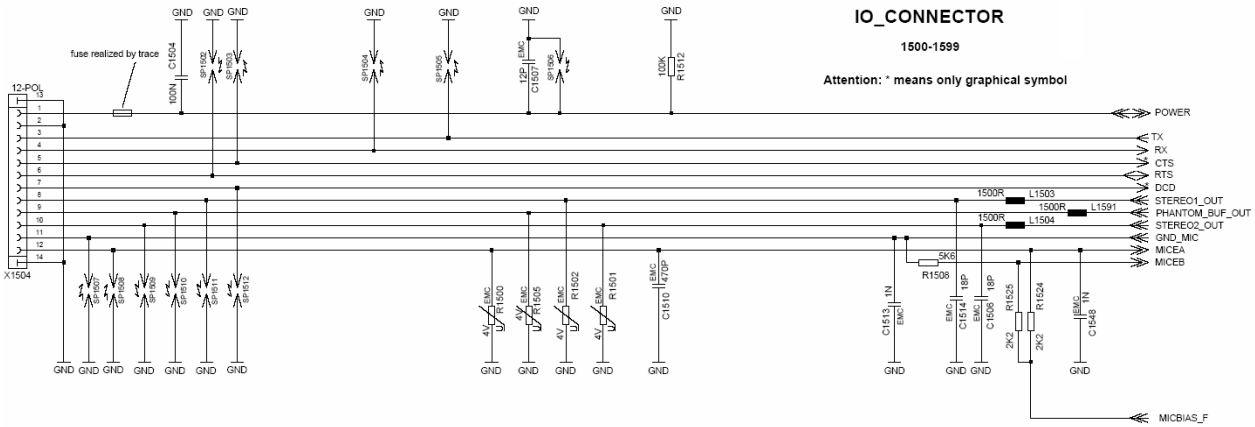


Pin Name	IN/OUT	Remarks
SIM_CLK	O	Pulse for chipcard. The SIM is controlled directly from the SGOLD.
SIM_RST	O	Reset for chipcard
SIM_IO	I/O	Data pin for chipcard
VDD_SIM	O	Switchable power supply for chipcard;

The Z1601 is a 3-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals. Additionally diodes are contained to protect downstream components from Electrostatic Discharge (ESD) voltages

15.4 IO Connector with ESD protection

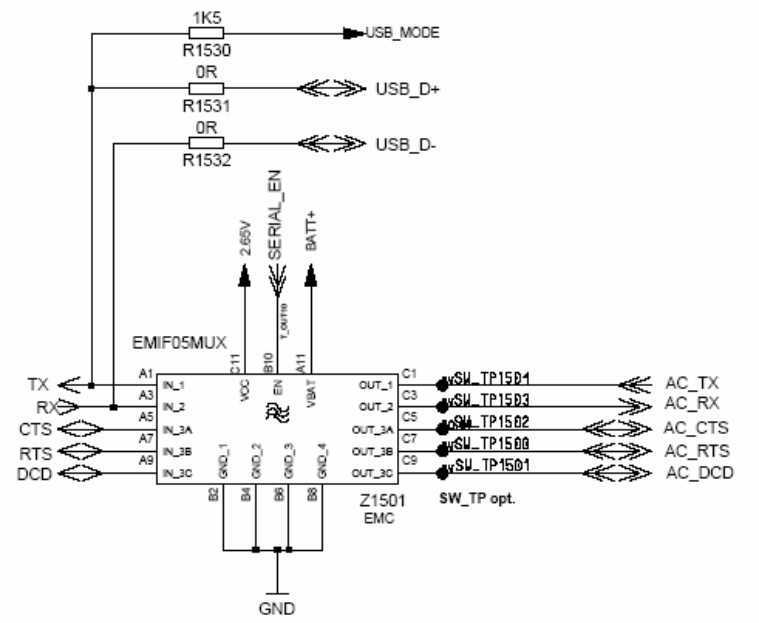
IO Connector – New Slim Lumberg



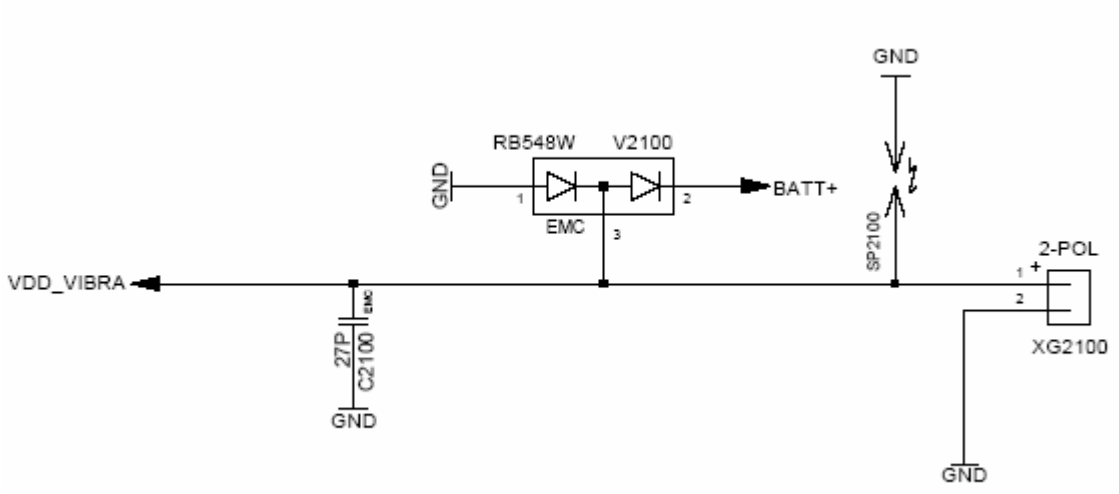
Pin	Name	IN/OUT	Notes
1	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
2	GND		
3	TX	O	Serial interface
4	RX	I	Serial interface
5	CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
6	RTS	I/O	Use as RTS in data-operation.
7	DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
8	STEREO1_OUT	Analog O	driving ext. left speaker to PHANTOM_BUF_OUT with mono-headset STEREO1_OUT and STEREO2_OUT differential mode
9	PHANTOM_BUF-OUT	Analog O	mid-voltage in stereo mode refernce to STEREO1_OUT and STEREO2_OUT in mono mode not used
10	STEREO2_OUT	Analog O	driving ext. right to PHANTOM_BUF_OUT with mono-headset STEREO1_OUT and STEREO2_OUT differential mode
11	GND_MIC	Analog I	for ext. microphone
12	MICEA	Analog I	External microphone

ESD Protection with EMI filter

The Z1501 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z1501 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages



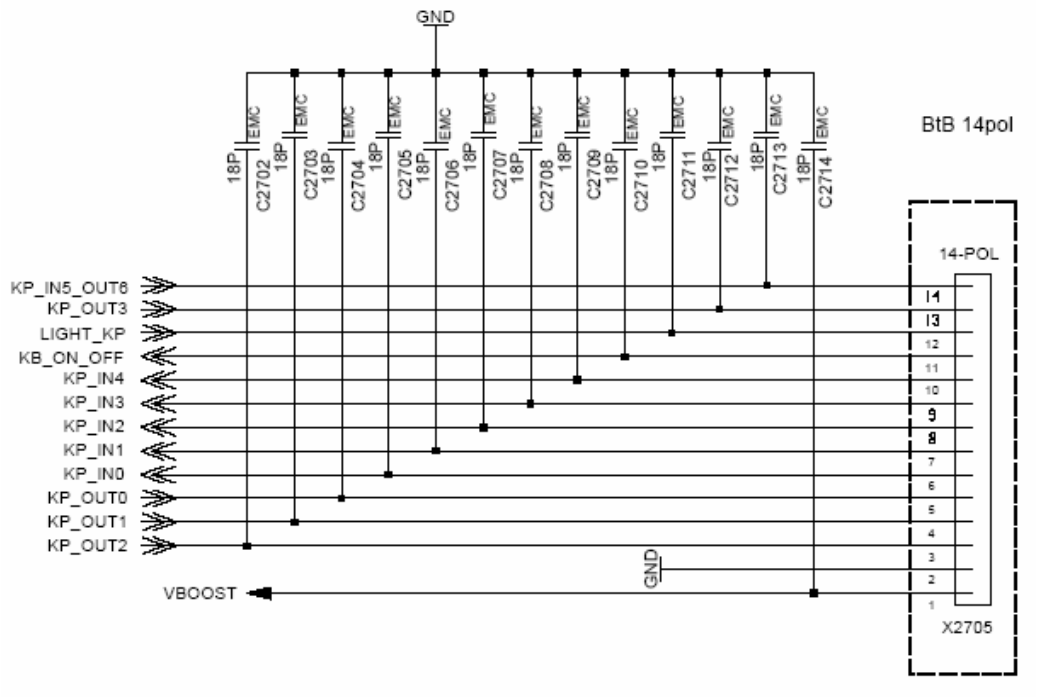
15.5 Vibration Motor (XG2100)



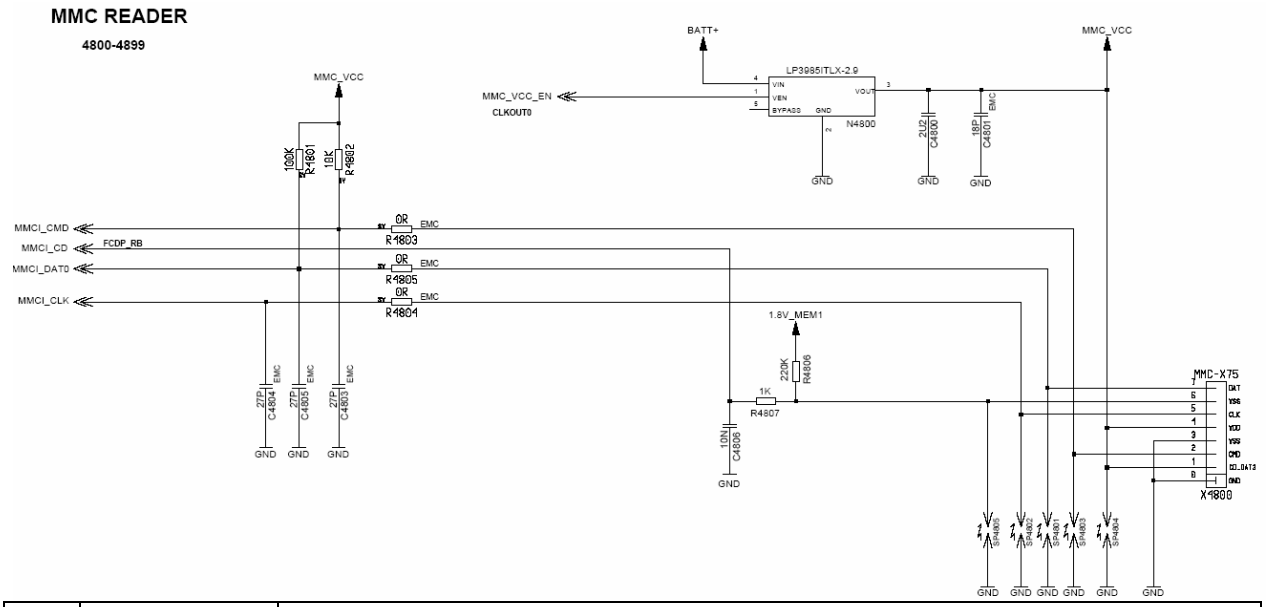
Pin	Name	IN/OUT	Remarks
1	VDD_VIBRA		Vbatt will be switched by PWM-signal with internal FET to VDD_Vibra in Asic
2	GND		

15.6 Board to Board Connector

Keyboard and keypad illumination are connected via an inter board connector (X2705).

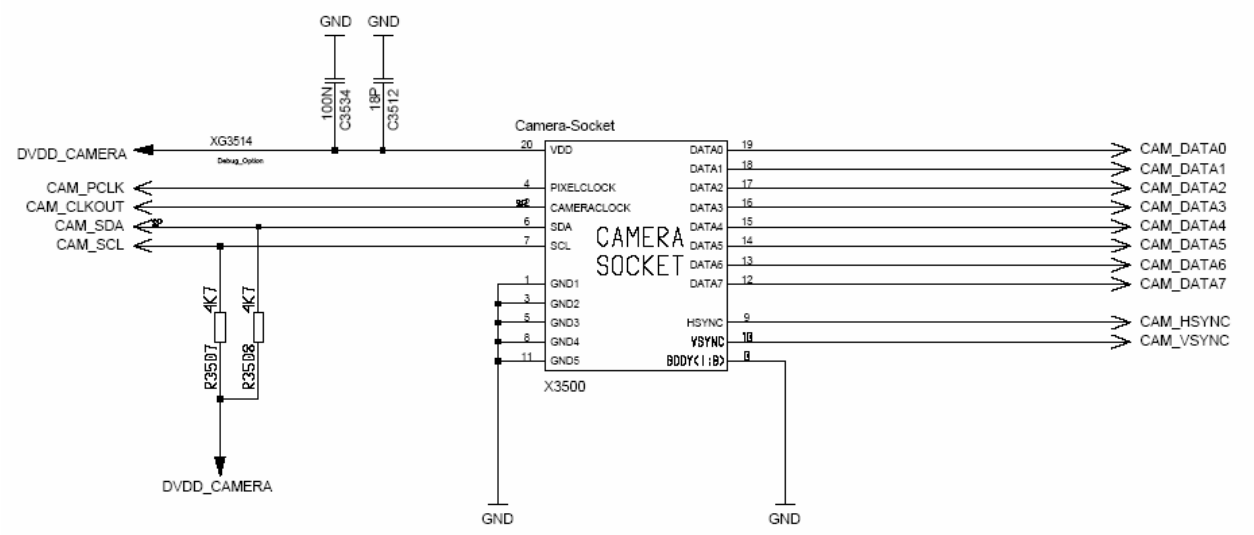


15.7 RSMMC Reader



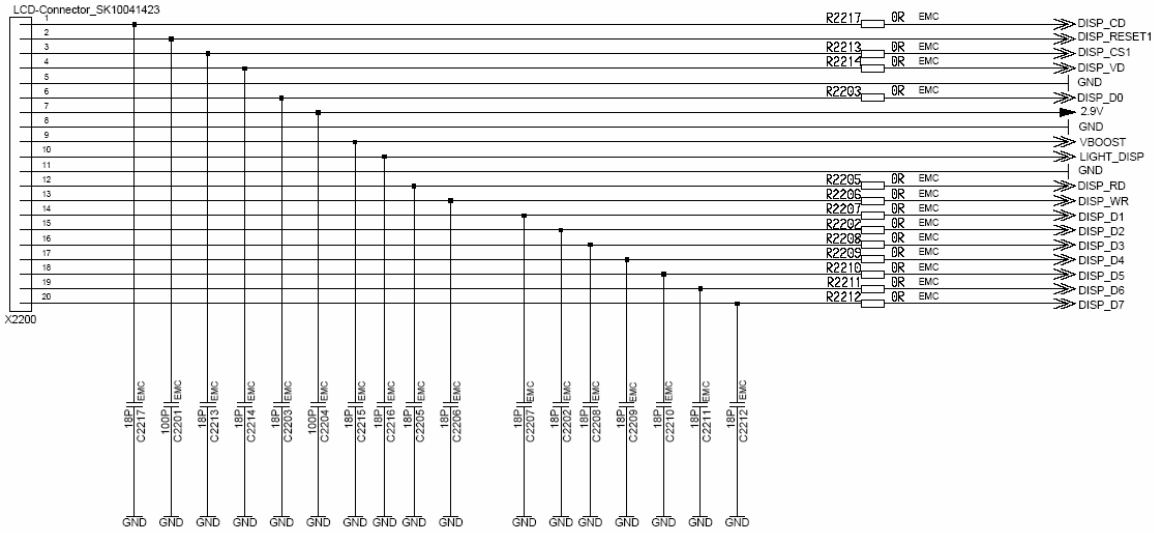
Pin	Name	Remarks
0	GND	Ground
1	MMC_VCC	Operating voltage MMC, 2.9V from N4800
2	MMC_CMD	MMC Command Line (“low” signal = read / ”high” signal =write) used only for initialisation
3	GND	Ground
4	MMC_VCC	Operating voltage MMC, 2.9V from N3580 (activated via MCC_VCC_EN)
5	MMC_CLK	MMC Clock Line
6	MMC_CD	MMC Card Detection Line
7	MMC_DAT	MMC Data Line

15.8 Camera Interface



Pin Number	Pin Name	Description	I/O
01	GND	Ground	N/A
02	EXCLK	Camera Clock	O
03	GND	Ground	N/A
04	Pixel Clock	Pixel Data Clock	I
05	GND	Ground	N/A
06	SDA	I2C Data	I/O
07	SCL	I2C Clock	O
08	GND	Ground	N/A
09	H_SYNC	Horizontal Synchronization	I
10	V_SYNC	Vertical Synchronization	I
11	GND	Ground	N/A
12	Data 7	Data bit 7	I
13	Data 6	Data bit 6	I
14	Data 5	Data bit 5	I
15	Data 4	Data bit 4	I
16	Data 3	Data bit 3	I
17	Data 2	Data bit 2	I
18	Data 1	Data bit 1	I
19	Data 0	Data bit 0	I
20	VDD	Supply Voltage 2,9V	N/A

15.9 Display Connector



Pin Nr.	Pin Name	Description
1	DISP_CD	Control / display data flag
2	DISP_RESET1	Reset (low active)
3	DISP_CS1	Chip select main display (low active)
4	DISP_VD	Tearing pin (synchronization of display refresh and data transmission)
5	GND	Power supply GND
6	DISP_D0	Parallel data bus
7	2.9V	Power supply V_{DD1}
8	GND	Power supply GND
9	VBOOST	Anode LED
10	LIGHT_DISP	Cathode LED
11	GND	Power supply GND
12	DISP_RD	Read selection parallel interface
13	DISP_WR	Write selection parallel interface
14	DISP_D1	Parallel data bus
15	DISP_D2	Parallel data bus
16	DISP_D3	Parallel data bus
17	DISP_D4	Parallel data bus
18	DISP_D5	Parallel data bus
19	DISP_D6	Parallel data bus
20	DISP_D7	Parallel data bus

16 M81 Diagram Sets

Double click the tag symbol to open the files.

TD_Repair_M81 Diagram Set_R1.0.pdf

TD_Repair_M81 Logic Diagram_R1.0.pdf

TD_Repair_M81_RF_ HIT_Diagram_R1.0.p