# Service Repair Documentation
# Level 3 CF110


| Release | Date | Department | Notes to change |
|---|---|---|---|
| R 1.0 | 29.11.2005 | BenQ Mobile CC S CES | New document |
| | | | |
| | | | |

# Table of Content

# 1 Introduction

## 1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3.

## 1.2 Scope

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Mobile mobile phones up to level 3.

## 1.3 Terms and Abbreviations

# 2 List of available level 3 parts

(according to Component Matrix V1.1 - check C-market for updates)

| Product | RF Chipset | ID | Order Number | Description CM |
|---|---|---|---|---|
| CF110 | HIT | D171 | L50610-L6150-D670 | IC EGOLDLITE PMB7860 |
| CF110 | HIT | D361 | L50645-J4682-Y55 | IC ASIC SALZBURG75 TWIGO3+75 |
| CF110 | HIT | D902 | L50645-K280-Y303 | IC FEM HITACHI GSM900 1800 1900 (Fem-Type5) |
| CF110 | HIT | D903 | L50620-L6170-D670 | IC TRANCEIVER HD155165BP PB Free |
| CF110 | HIT | L1302 | L36151-F5103-M7 | COIL 10U (Co-Type2) |
| CF110 | HIT | L1303 | L36140-F2100-Y6 | COIL 0603 (Co-Type4) |
| CF110 | HIT | N1304 | L36820-C6250-D670 | IC DC DC BOOST CONVERTER |
| CF110 | HIT | N308 | L506810-C6153-D670 | IC ANA RE 2.9V USMD5 PB FREE |
| CF110 | HIT | N901 | | IC MODUL PA PF0814 (PA-Type3) PB Free |
| CF110 | HIT | S851 | L36197-F5008-F63 | IC PER HALL SENSOR (Hs-Type1) |
| CF110 | HIT | S852 | L36197-F5008-F63 | IC PER HALL SENSOR (Hs-Type1) |
| CF110 | HIT | V1303 | L36840-D5076-D670 | DIODE SOD323 (Di-Type7) |
| CF110 | HIT | V1400 | L36840-D66-D670 | DIODE BAV99T (Di-Type5) |
| CF110 | HIT | V211 | L36830-C1097-D670 | TRANSISTOR FDG313N (Tra-Type1) |
| CF110 | HIT | V220 | L36851-Z9105-Z981 | DIODE 1SS355 (Di-Type6) |
| CF110 | HIT | V222 | L36840-C4014-D670 | TRANSISTOR BC847BS BC846S (Tra-Type7) |
| CF110 | HIT | V2302 | L36840-C4014-D670 | TRANSISTOR BC847BS BC846S (Tra-Type7) |
| CF110 | HIT | V2303 | L36840-C4014-D670 | TRANSISTOR BC847BS BC846S (Tra-Type7) |
| CF110 | HIT | V361 | L36830-C1110-D670 | TRANSISTOR SI3911 (Tra-Type3) |
| CF110 | HIT | X3800 | L36334-Z97-C334 | CONNECTOR COAX SOCKET SWITCHED |
| CF110 | HIT | Z171 | L50645-F102-Y40 | QUARZ 32,768KHZ (Q-Type4) |
| CF110 | HIT | Z211 | L50640-U6034-D670 | FILTER EMI (Fi-Type3) PB Free |

# 3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A1)
- Troubleshooting Frame CF110 (F30032-P588-A1)
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

*Reference:* Equipment recommendation V1.6
(downloadable from the technical support page)

# 4 Required Software for Level 3

- Windows XP
- X-Focus version 1.68 or higher
- GRT Version 3 or higher
- Internet unblocking solution (JPICS)

# 5 Radio Part

The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

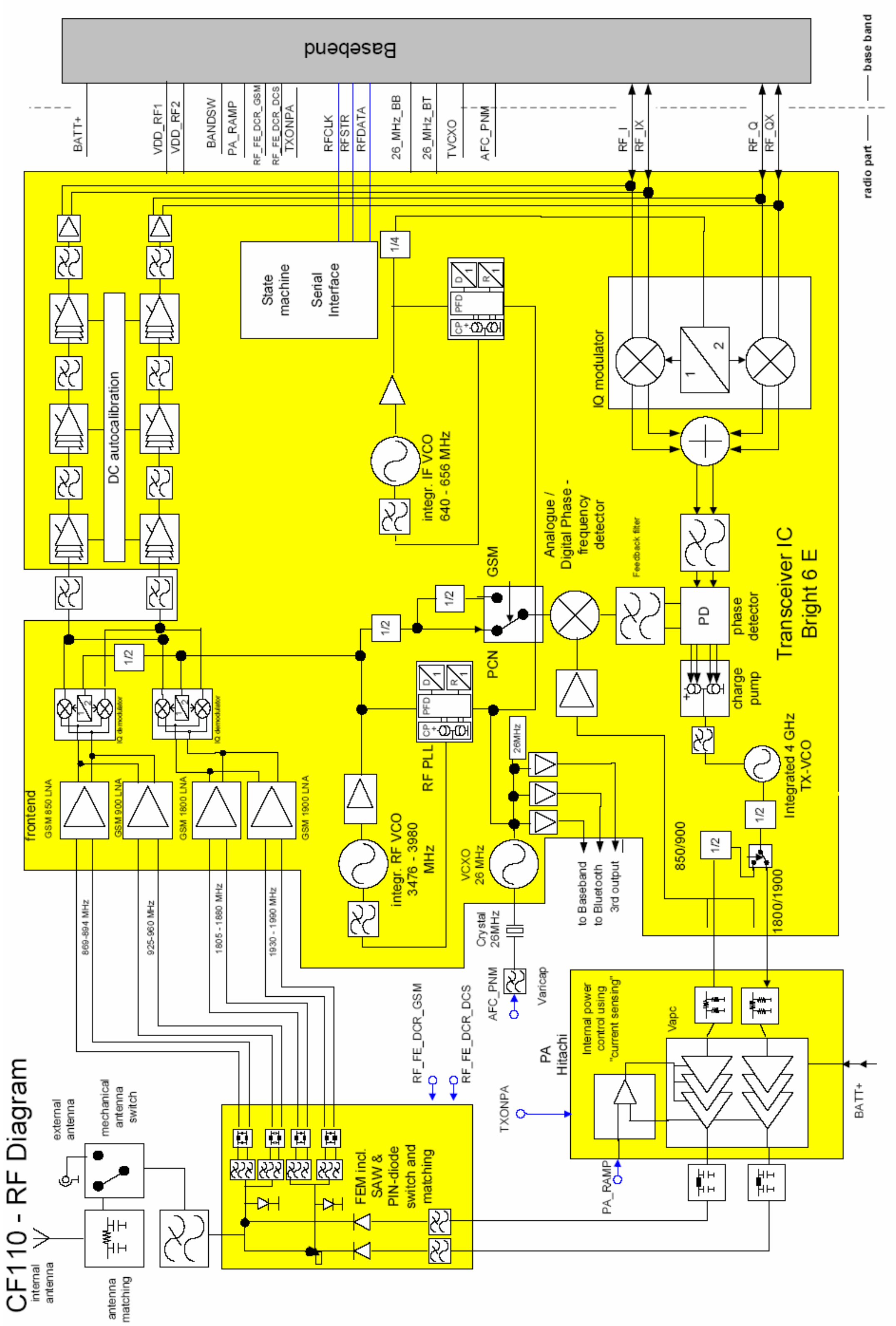
Transmitter and Receiver are never active at the same time. Simultaneous receiving in the EGSM900 and GSM1800 band is impossible. Simultaneous transmission in the EGSM900 and GSM1800 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

The RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000) supporting GPRS functionality up to multiclass 8.

The RF-circuit consists of the following components:

- Hitachi Bright VI E chip set (HD155165BP) with the following functionality:
    - PLL for local oscillator LO1 and LO2 and TxVCO
    - Integrated local oscillators LO1, LO2
    - Integrated TxVCO
    - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
    - 26 MHz reference oscillator
- Hitachi LTCC transmitter power amplifier with integrated power control circuitry
- Hitachi Frontend-Module including RX-/TX-switch and EGSM900 / DCS1800 / PCS 1900 receiver SAW-filters
- Quartz and passive circuitry of the 26MHz VCXO reference oscillator

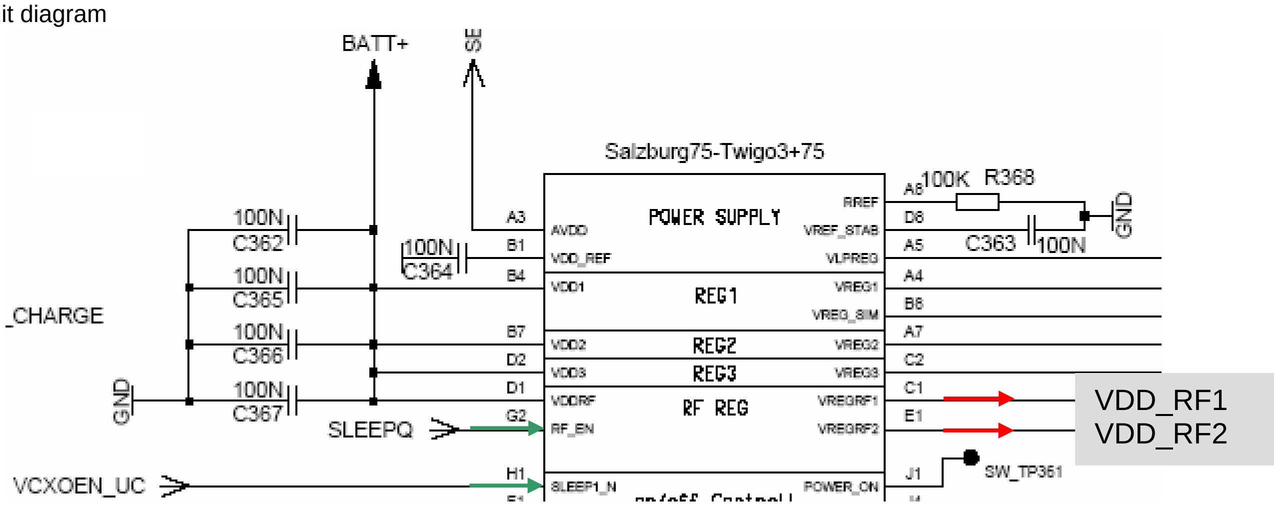
## 5.1 Block diagram RF part

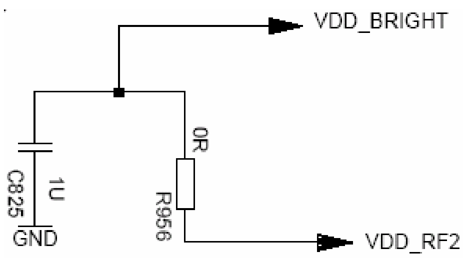


## 5.2 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D361.It generates the required 2,8V “RF-Voltages” named VDD_RF1 and VDD_RF2. VDD_RF2 is passed via a 0Ω resistor and renamed as VDD_BRIGHT as operating voltage for the BRIGHT. The voltage regulator is activated as well as deactivated via SLEEPQ (TDMA-Timer R11) and VCXOEN_UC (M4) provided by the EGOLDlite. The temporary deactivation is used to extend the stand by time.

Circuit diagram




## 5.3 Frequency generation

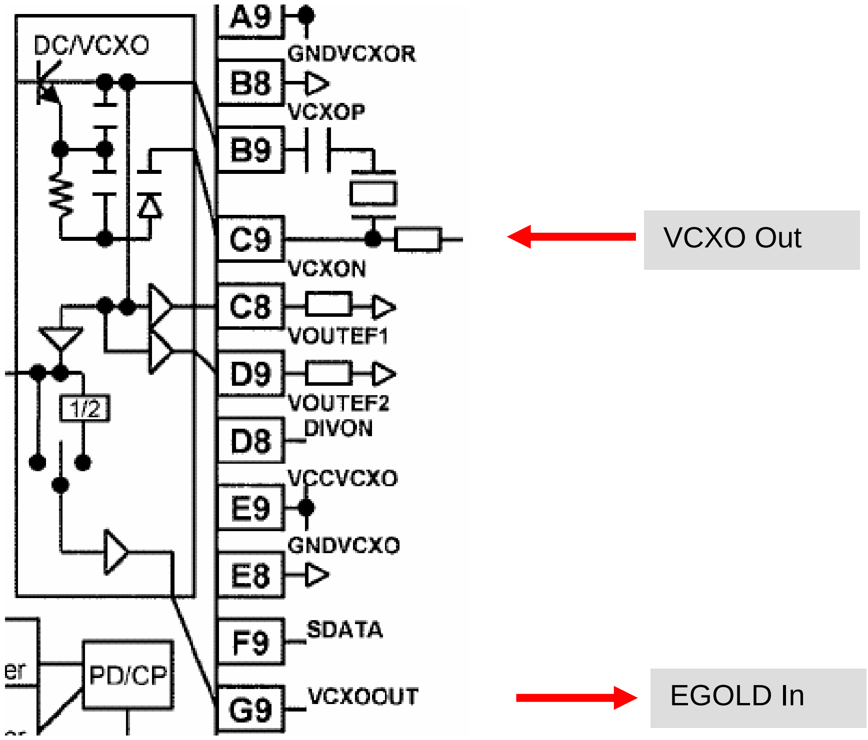
Synthesizer: The discrete VCXO (26MHz)

The AX75 mobile is using a reference frequency of 26MHz. The generation of the 26MHz signal is done via a VCO (Z950).

TP (test point) of the 26MHz signal is the TP 820

The oscillator output signal 26MHz_RF is directly connected to the BRIGHT IC (ball B9,. C9) to be used as reference frequency inside the Bright (PLL). The signal leaves the Bright IC as RF_SIN26M (ball G9) to be further used from the EGOLDlite (D171 (C8)).

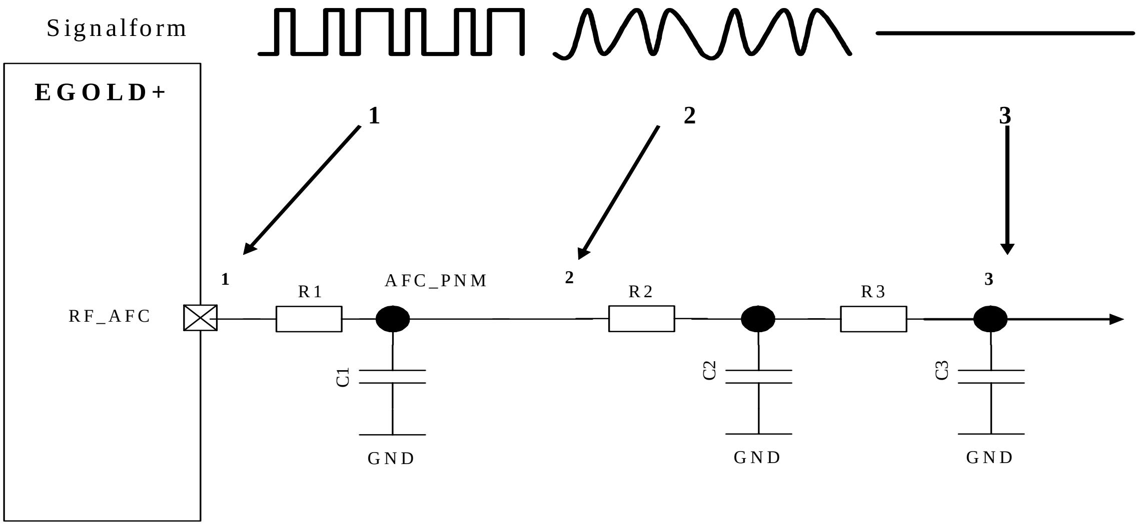
Bright 6E




To compensate frequency drifts (e.g. caused by temperature) the oscillator frequency is controlled by the (RF_AFC) signal, generated through the internal EGOLDlite (D171 (A10)) PLL. Reference for the "EGOLD-PLL" is the base station frequency received via the Frequency Correction Burst.

The required voltage VDD_RF2 is provided by the ASCI D361

**Waveform of the AFC_PNM signal from EGOLDlite to Oscillator**

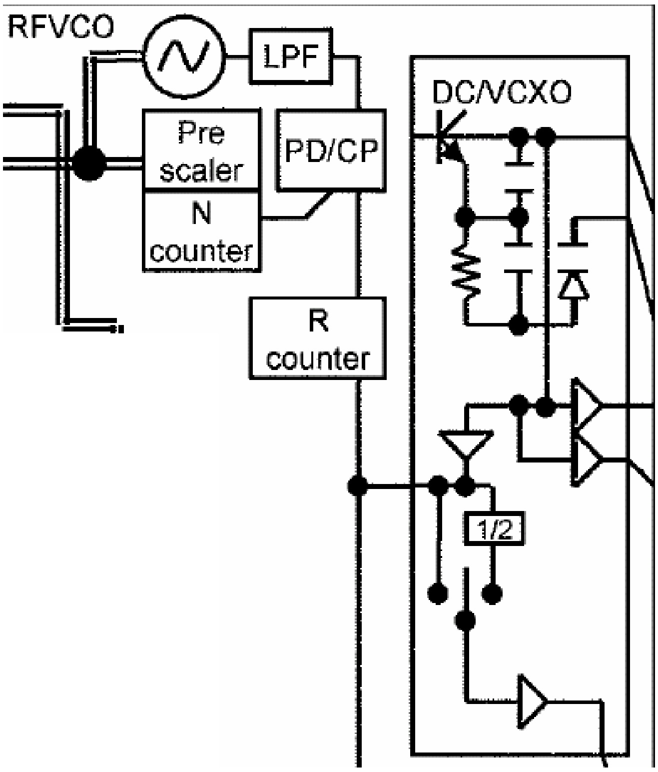


Synthesizer: LO1

First local oscillator (LO1) consists of a PLL and VCO inside Bright (D903) and an internal loop filter

RF PLL
The frequency-step is 400 kHz in GSM1800 mode and 800kHz in EGSM900 mode due to the internal divider by two for GSM1800 and divider by four for EGSM900. To achieve the required settling-time in GPRS operation, the PLL can operate in fastlock-mode a certain period after programming to ensure a fast settling. After this the loopfilter and currents are switched into normal-mode to get the necessary phasenoise-performance. The PLL is controlled via the tree-wire-bus of Bright VI E.

RFVCO (LO1)
The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The VCO module is switched on with the signal PLLON. The full oscillation range is divided into 256 sub-bands To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the EGOLDlite, according to the network channel requirements.



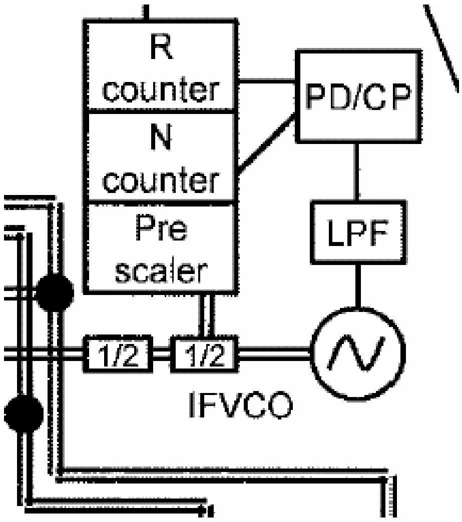
Matrix to calculate the TX and RX frequencies AX75:

| **Band** | **RX / TX** | **Channels** | **RF frequencies** | **LO1 frequency** | **IF freq.** |
|---|---|---|---|---|---|
| EGSM 900 | Receive: | 0..124 | 935,0 - 959,8 MHz | LO1 = 4*RF | |
| EGSM 900 | Transmit: | 0..124 | 890,0 - 914,8 MHz | LO1 = 4*(RF+IF) | 80,0 MHz |
| EGSM 900 | Receive: | 975..1023 | 925,2 - 934,8 MHz | LO1 = 4*RF | |
| EGSM 900 | Transmit: | 975..1023 | 880,2 - 889,8 MHz | LO1 = 4*(RF+IF) | 82,0 MHz |
| GSM 1800 | Receive: | 512..661 | 1805,2 - 1835,0 MHz | LO1 = 2*RF | |
| GSM 1800 | Transmit: | 512..661 | 1710,2 - 1740,0 MHz | LO1 = 2*(RF+IF) | 80,0 MHz |
| GSM 1800 | Receive: | 661..885 | 1835,0 - 1879,8 MHz | LO1 = 2*RF | |
| GSM 1800 | Transmit: | 661..885 | 1740,0 - 1784,8 MHz | LO1 = 2*(RF+IF) | 82,0 MHz |
| GSM 1900 | Receive: | 512..810 | 1930,2 - 1989,8 MHz | LO1 = 2*RF | |
| GSM 1900 | Transmit: | 512..810 | 1850,2 - 1909,8 MHz | LO1 = 2*(RF+IF) | 80,0 MHz |

Synthesizer: LO2

The second local oscillator (LO2) consists of a PLL and VCO inside Bright (D903) and an internal loop filter. Due to the direct conversion receiver architecture, the LO2 is only used for transmit-operation. The LO2 covers a frequency range of at least 16 MHz (640MHz – 656MHz).
Before the LO2-signal gets to the modulator it is divided by 8. So the resulting TX-IF frequencies are 80/82 MHz (dependent on the channel and band). The LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (EGOLDLite signals RF_DAT; RF_CLK; RF_STR). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2$^{nd}$ PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

The required voltage VDD_BRIGHT is provided by the ASIC D361

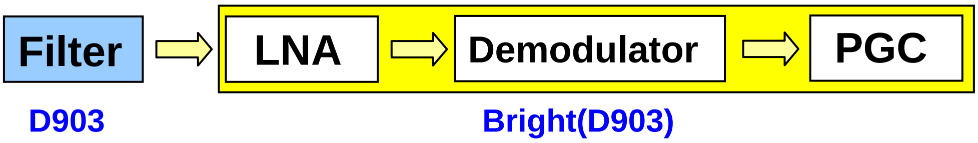


## 5.4 Receiver

Receiver: Filter to Demodulator

The band filters are located inside the frontend module (D902). The filters are centred to the band frequencies. The symmetrical filter output is matched to the LNA input of the Bright .The Bright 6E incorporates three RF LNAs for GSM850/EGSM900, GSM1800 and GSM1900 operation. The LNA/mixer can be switched in High- and Low-mode to perform an amplification of ~ 20dB. For the “High Gain“ state the mixers are optimised to conversion gain and noise figure, in the “Low Gain“ state the mixers are optimised to large-signal behavior for operation at a high input level. The Bright performs a direct conversion mixers which are IQ-demodulators. For the demodulation of the received GSM signals the LO1 is required. The channel depending LO1 frequencies for 1800MHz/1900MHz bands are divided by 2 and by 4 for 850MHG/900MHz band. Furthermore the IC includes a programmable gain baseband amplifier PGA (90 dB range, 2dB steps) with automatic DC-offset calibration. LNA and PGA are controlled via EGOLDlite signals RF_DAT; RF_CLK; RF_STR**(RF Contr N6, R6, N4)**. The channel-filtering is realized inside the chip with a three stage baseband filter for both IQ chains. Only two capacitors which are part of the first passive RC-filters are external. The second and third filters are active filters and are fully integrated. The IQ receive signals are fed into the A/D converters in the EGAIM part of EGOLDlite. The post-switched logic measures the level of the demodulated baseband signal and regulates the level to a defined value by varying the PGA amplification and switching the appropriate LNA gains.

From the antenna switch, up to the demodulator the received signal passes the following blocks to get the demodulated baseband signals for the EGOLDlite:

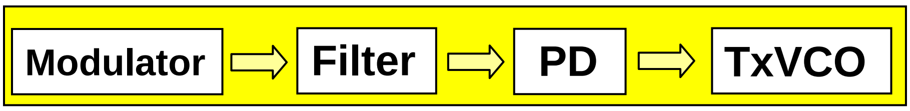



The required voltage VDD_BRIGHT is provided by the ASIC D361

## 5.5 Transmitter

Transmitter: Modulator and Up-conversion Loop

The generation of the GMSK-modulated signal in Bright (D903) is based on the principle of up conversion modulation phase locked loop. The incoming IQ-signals from the baseband are mixed with the divided LO2-signal. The modulator is followed by a lowpass filter (corner frequency ~80 MHz) which is necessary to attenuate RF harmonics generated by the modulator. A similar filter is used in the feedback-path of the down conversion mixer.
With help of an offset PLL the IF-signal becomes the modulated signal at the final transmit frequency. Therefore the GMSK modulated rf-signal at the output of the TX-VCOs is mixed with the divided LO1-signal to a IF-signal and sent to the phase detector. The I/Q modulated signal with a center frequency of the intermediate frequency is send to the phase detector as well.
The output signal of the phase detector controls the TxVCO and is processed by a loop filter whose components are external to the Bright. The TxVCO which is realized inside the Bright chip generates the GSMK modulated frequency.



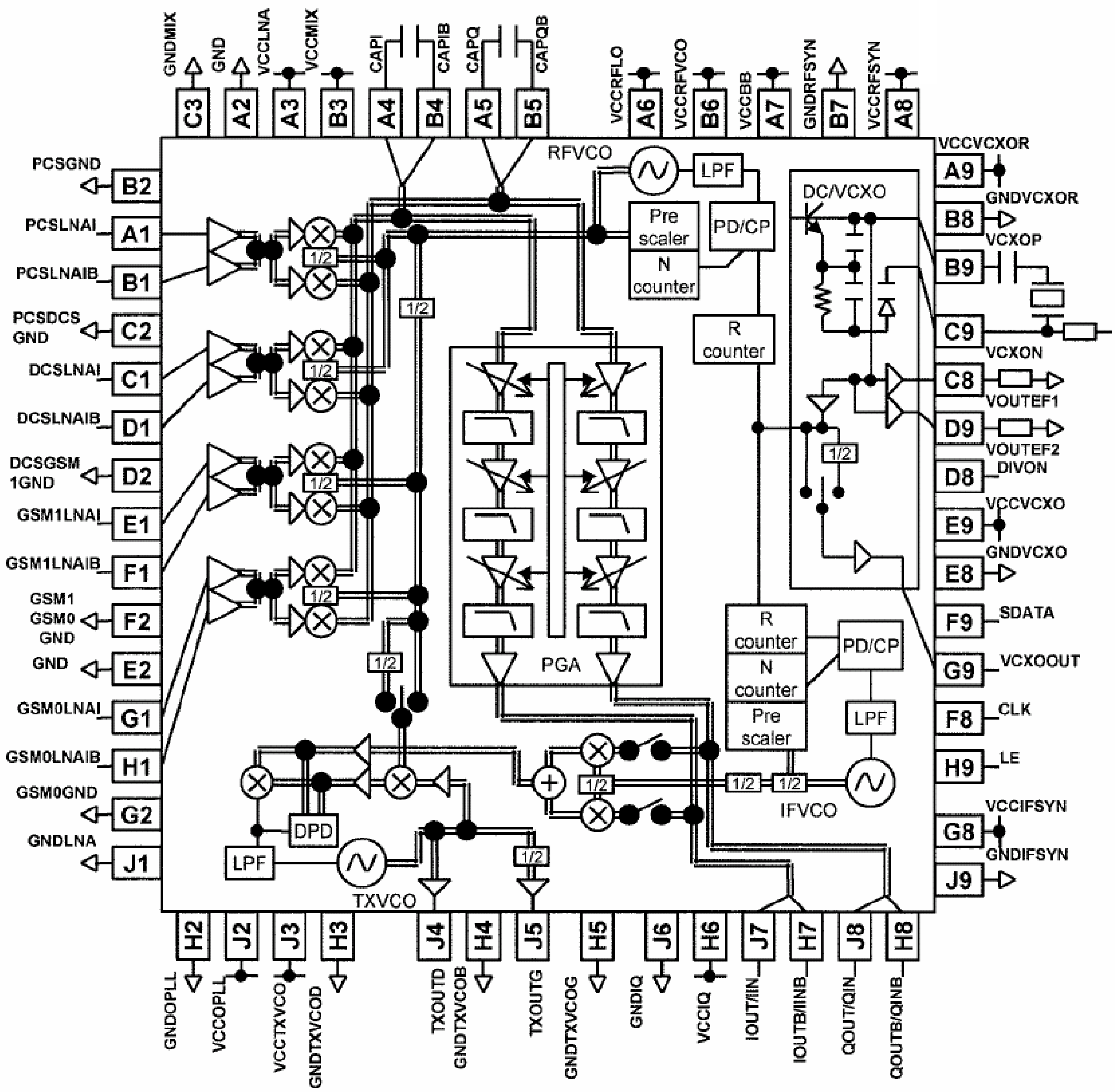

**Bright(D903)**

The required voltage VDD_BRIGHT is provided by the ASIC D361

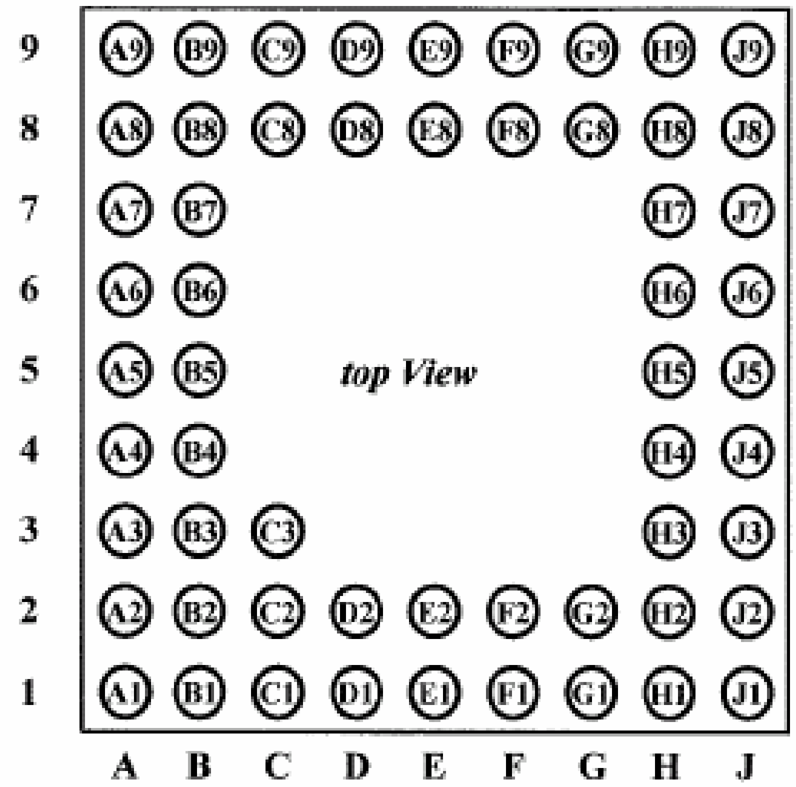
## 5.6 Bright IC Overview

BRIGHT 6E

IC Overview



IC top view (ball overview)



## 5.7 Antenna switch (electrical/mechanical)

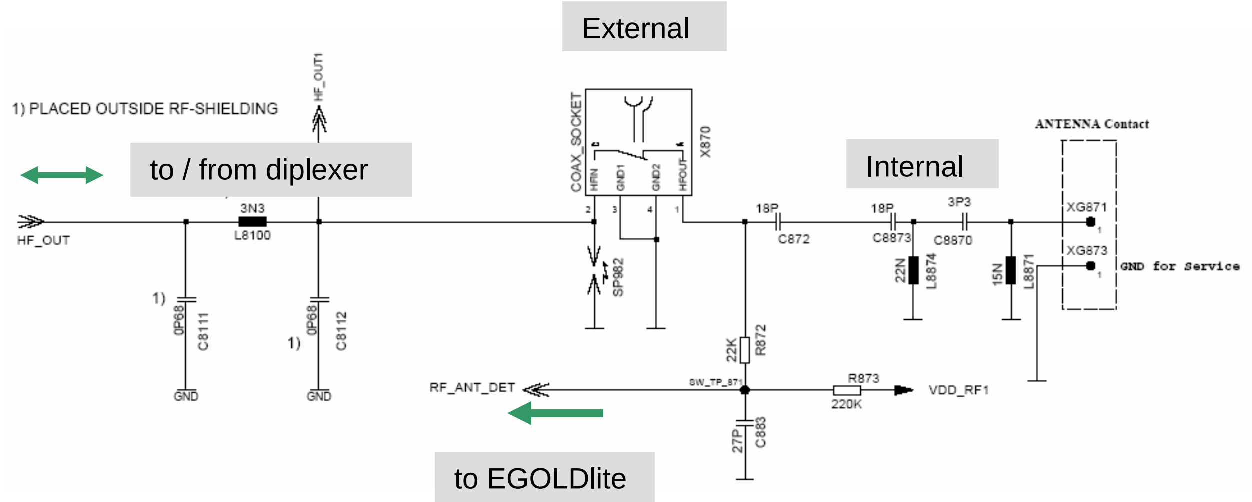
Internal/External <> Receiver/Transmitter
The A70 mobile have two antenna switches.

a) The mechanical antenna switch for the differentiation between the internal and external antenna which is used only for RF adjustments on the board.

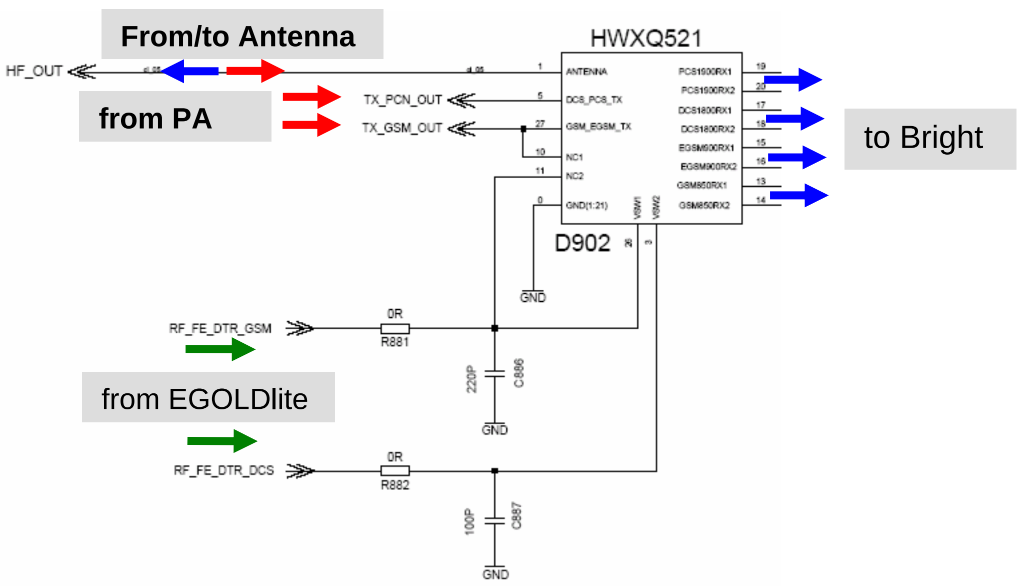
b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals.

To activate the correct tx pathes of this diplexer, the EGOLDlite signals RF_FE_DTR_GSM and RF_FE_DTR_DCS are required.

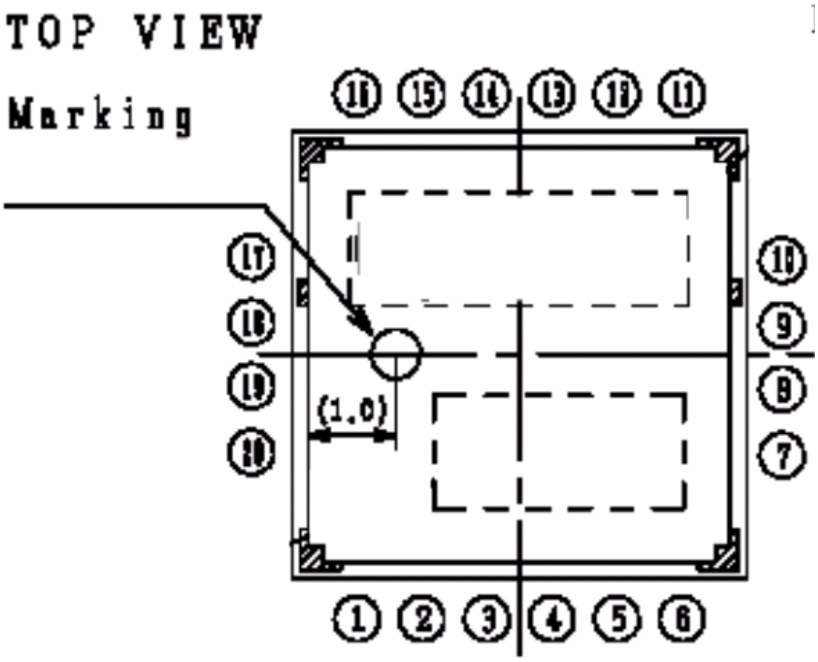
Internal/External antenna switch




The electrical antenna switch



Top View :




Switching Matrix:

| select mode | Vsw 1 | Vsw 2 |
|---|---|---|
| GSM900/DCS1800/PCS1900 RX | Low | Low |
| EGSM TX | high | Low |
| DCS1800/PCS1900 TX | Low | High |

Pin assignment:

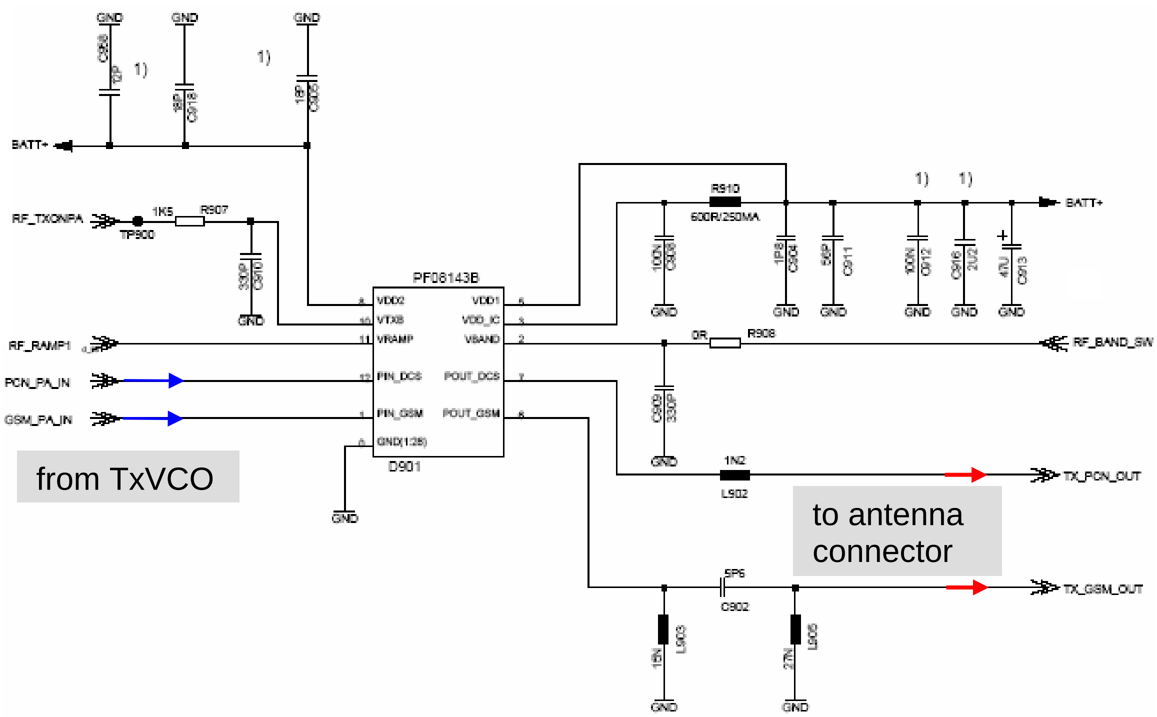
| | | | |
|---|---|---|---|
| 1 | Antenna | 15 | PCS1900 RX1 |
| 2 | GND | 16 | PCS1900 RX2 |
| 3 | Vsw2 (DCS1800/PCS1900 TX control) | 17 | GND |
| 4 | GND | 18 | GND |
| 5 | DCS1800/PCS1900 TX | 19 | GND |
| 6 | GND | 20 | GND |
| 7 | GND | 21 | GND |
| 8 | EGSM900 TX | 22 | GND |
| 9 | Vsw1 (EGSM900 TX control) | 23 | GND |
| 10 | GND | 24 | GND |
| 11 | EGSM900 RX1 | 25 | GND |
| 12 | EGSM900 RX2 | 26 | GND |
| 13 | DCS1800 RX1 | 27 | GND |
| 14 | DCS1800 RX2 | 28 | GND |

## Transmitter: Power Amplifier

The output signals (PCN_PA_IN , and GSM_PA_IN) from the TxVCO are led to the power amplifier. The power amplifier is a PA-module N901 from Hitachi. It contains two separate 3-stage amplifier chains GSM850/EGSM900 and GSM1800 / GSM1900 operation. It is possible to control the output-power of both bands via one VAPC-port. The appropriate amplifier chain is activated by a logic signal RF_BAND_SW (TDMA Timer P10) which is provided by the EGOLDLite.
To ensure that the output power and burst-timing fulfills the GSM-specification, an internal power control circuitry is use. The power detect circuit consists of a sensing transistor which operates at the same current as the third RF-transistor. The current is a measure of the output power of the PA. This signal is square-root converted and converted into a voltage by means of a simple resistor. It is then compared with the RF_RAMP1 (F12) signal.
The N901 is activated through the signal RF_TXONPA (TDMA Timer P3).

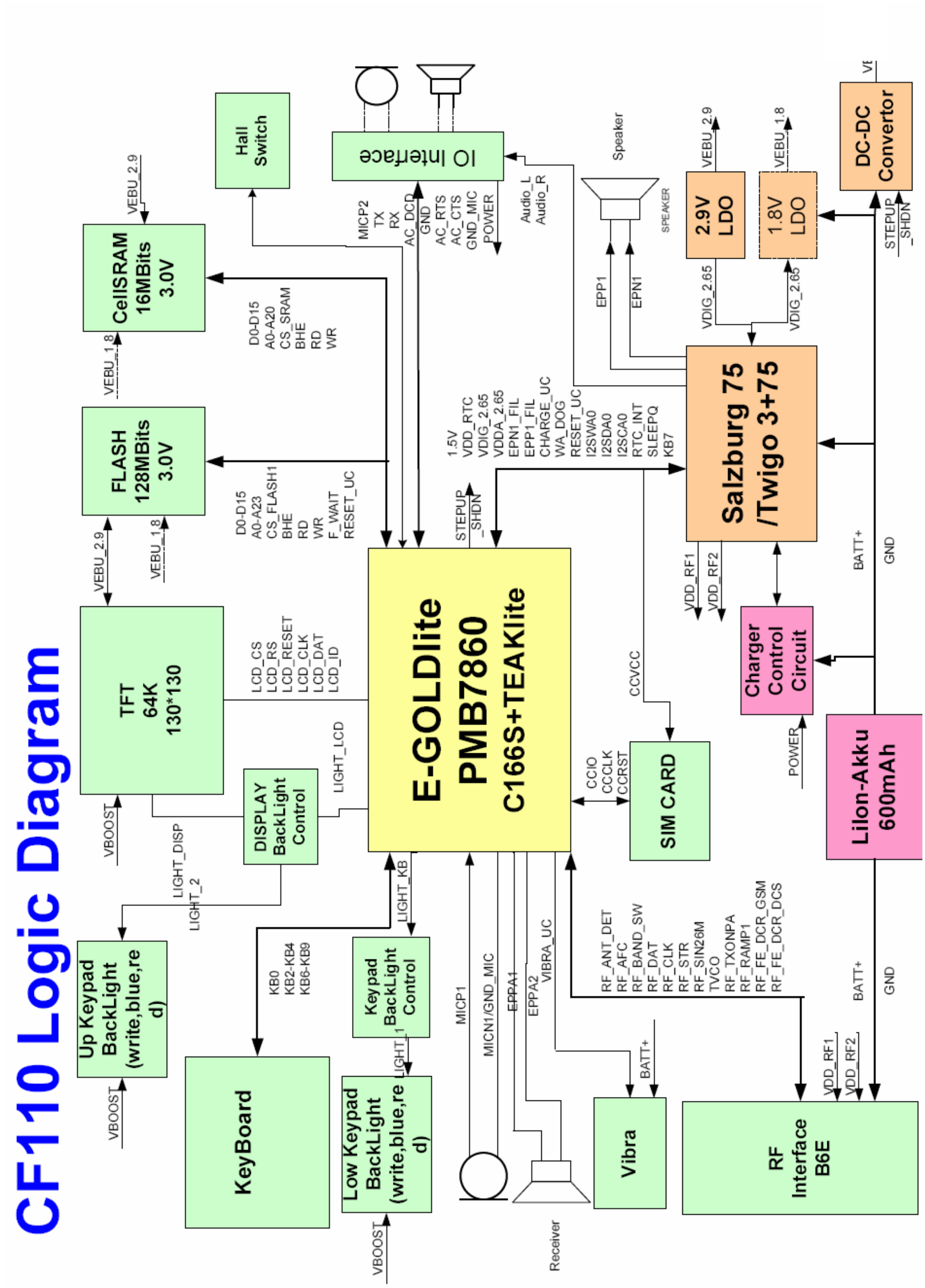
The required voltage BATT+ is provided by the battery.

Circuit diagram



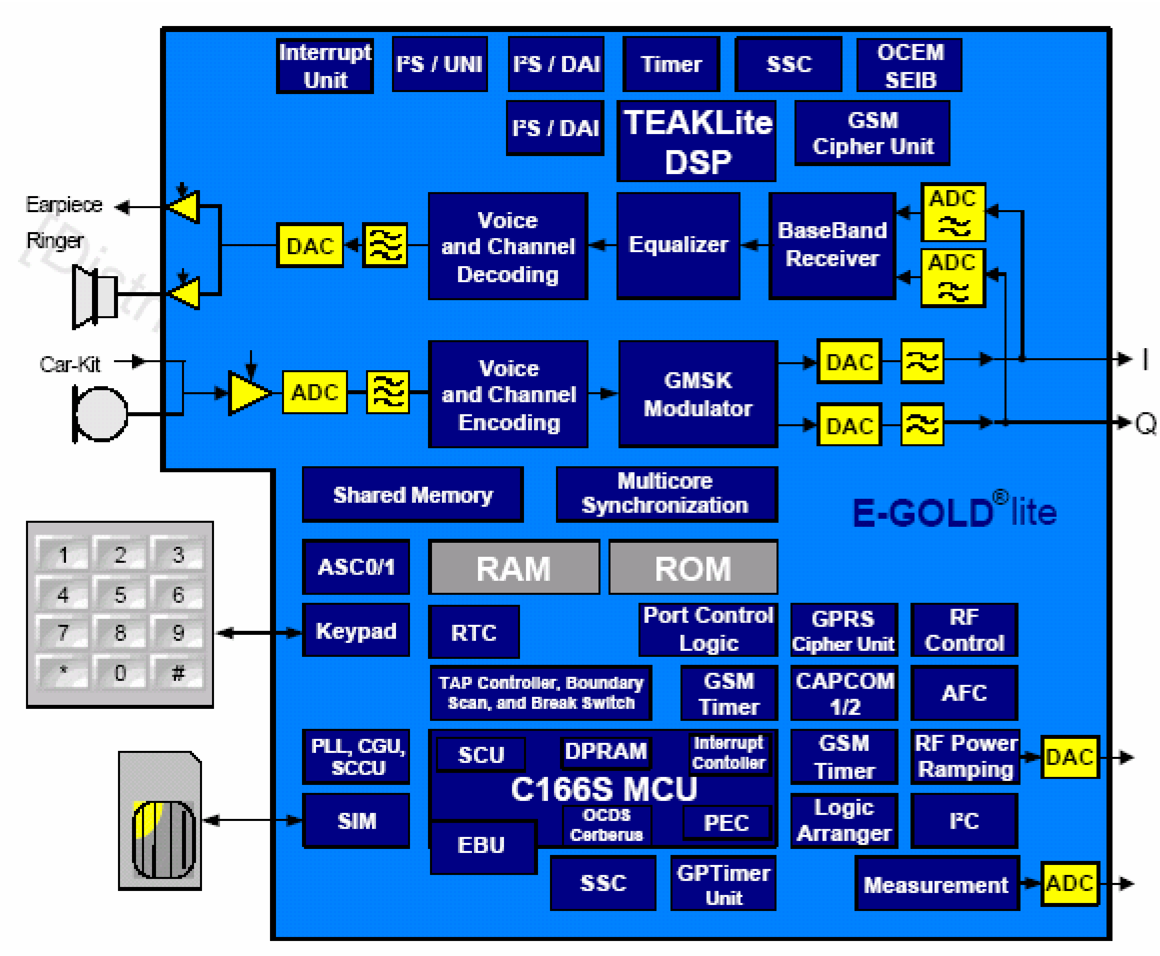
# 6 Logic / Control

## 6.1 Overview of Hardware Structure CF110



## 6.2 EGOLDlite

### Blockdiagram EGOLDlite



E-GOLDlite is designed as a single chip solution that integrates the digital and mixed signal portions of the baseband. It uses a leading 0.13 µm technology with a core voltage of 1.5 V. This allows and high performance mobile station with a large set of features at very low cost.
E-GOLDlite has a flexible set of interfaces that allows a wide choice of communication interfaces and supports a high multimedia data rate.

E-GOLDlite is powered by C166®S CPU and TEAKLite® DSP cores.

The E-GOLDlite is placed in a S-LF2BGA201 (a “flipchip” with 201 pins) with 0,5mm Ball-Pitch.

The E-GOLDlite is suited for mobile stations operating in the GSM850/900/1800/1900 bands.

In the receiver path the antenna input signal is converted to the base band, filtered, and amplified to target level by the RF transceiver chipset. The resulting differential I and Q baseband signals are fed into the E-GOLDlite. The A-to-D converter generates two 6.5 Mbit/s data streams. The decimation and narrowband channel filtering is done by a digital baseband filter in each path. The DSP performs:
1. The GMSK equalization of the received baseband signal.
2. Channel decoding, which is supported by an hardware accelerator.

The recovered digital speech data is fed into the speech decoder. The E-GOLDlite supports fullrate, halfrate, enhanced fullrate and adaptive multirate speech CODEC algorithms.

The generated voice signal passes through a digital voiceband filter. The resulting 4 Mbit/s data stream is D-to-A converted by a multi-bit-oversampling converter, postfiltered, and amplified by a programmable gain stage.

The output buffer can drive a handset ear-piece or an external audio amplifier.

In the transmit direction the microphone signal is fed into a programmable gain amplifier. The prefiltered and A-to-D converted voice signal forms a 2 Mbit/s data stream. The oversampled voice signal passes a digital decimation filter.

Speech and channel encoding (including voice activity detection (VAD) and discontinuous transmission (DTX)) as well as digital GMSK modulation is carried out by the EGOLDlite.

The digital I and Q baseband components of the GMSK modulated signals (48-times oversampled with 13 MSamples/s) are D-to-A converted. The analog differential baseband signals are fed into the RF transceiver chipset.

The RF transceiver modulates the baseband signal to the desired frequency in the 850 MHz, 900 MHz, 1.8 GHz, and 1.9 GHz band using an I/Q modulator. The E-GOLDlite is able to support quad band applications.

Finally, an RF power module amplifies the RF transmit signal to the required power level. Using software, the E-GOLDlite controls the gain of the power amplifier by predefined ramping curves (16 words, 11 bits). The E-GOLDlite communicates with the RF chip set via a serial data interface.

The E-GOLDlite also includes battery charger support (various sensor connections for temperature, battery technology, voltage, etc.) and a ringer buffer.

For base band operation, the E-GOLDlite supports:
• High Speed Circuit Switched Data (HSCSD) class 4
• Packet-oriented data (GPRS) class 4 with a coding scheme from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.

If the E-GOLDlite is only used as a modem, then it supports:

• High Speed Circuit Switched Data (HSCSD) class 10
Note: With a HSCSD class 10, there are a maximum of 4 received time slots and 2 transmitted time slots.
The total maximum number of received and transmitted time slots is 5.

• Packet-oriented data (GPRS) class 10 with a coding scheme from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.
Note: With a GPRS class 10, there are a maximum of 4 received time slots and 2 transmitted time slots.
The total maximum number of received and transmitted time slots is 5.

The E-GOLDlite can support Class B operation. The mobile phone can be attached to both GPRS and GSM services, using one service at a time. During a GPRS connection Class B enables either:

• Making or receiving a voice call
• Sending or receiving an SMS.

During voice calls or SMS, GPRS services are suspended and then resumed automatically after the call or SMS session has ended.

E-GOLDlite is made with the Infineon C11N process using the High Voltage Threshold (HVT) and 5 Metal Layer (5LM).

The C11N process is a 0.13 µm technology. It is used for the logic, SRAM, mixed signal, and mixed voltage Input/Output applications.

## C166S MCU

The C166S is a 16-bit CMOS (Complementary Metal Oxide Silicon) microcontroller. It contains a CPU (Central Processing Unit) core (the MCU) and a set of peripherals.

The architecture of the MCU combines both RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) architecture.

• High Performance 16-Bit MCU with a four-stage pipeline:
  – 38 ns minimum instruction cycle time with most instructions executed in 1 cycle (2 clock ticks)
  – 192 ns multiplication (16-bit x 16-bit), 384 ns division (32-bit/16-bit)
  – Parallel use of multiple high bandwidth internal data buses
  – Register based design with multiple variable register banks
    – Single cycle context switching support
  – 16 MBytes linear address space for code and data (von Neumann architecture)
  – System stack cache support with automatic stack overflow/underflow detection.

• Control Oriented Instruction Set with High Efficiency:
  – Bit, byte, and word data types
  – Flexible and efficient addressing modes for high code density
  – Enhanced boolean bit manipulation with direct addressing of 6 Kbits for peripheral
  • control and user defined flags
  – Hardware traps to identify exception conditions during runtime
  – HLL support for semaphore operations and efficient data access.
• External Bus Interface:
  – Demultiplexed bus configurations
  – Segmentation capability and chip select signal generation
  – 8-bit or 16-bit data bus
  – Bus cycle characteristics selectable for five programmable address areas.
• 16-Priority-Level Interrupt System:
  – Up to 112 interrupt nodes with separate interrupt vectors
  – 16 priority levels and 8 group levels.
• 16-Channel Peripheral Event Controller (PEC):
  – Interrupt driven single cycle data transfer
  – Transfer count option (standard MCU interrupt after programmable number of PEC transfers)
  – Long Transfer Counter
  – Channel Linking
  – Eliminates overhead for saving and restoring system state for interrupt requests.

- DPRAM:
  - Internal 16-bit dual port RAM with a 1K x 16-bit size.
- SCU (System Control Unit):
  - Handles the boot and sleep mode of the core
  - Provides a watchdog timer.

The architecture of the C166S combines the advantages of both RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) processors in a well-balanced way. C166S based derivatives not only integrate a powerful MCU (Central Processing Unit) core and a set of peripheral units into one chip, but also connects the units in a very efficient way. One of the four buses used concurrently on the C166S is the Internal Bus Interface, an internal representation of the external bus interface. This bus provides a standardized method of integrating application-specific peripherals to produce derivatives of the standard C166S.

The Principle Elements of a C166S Based System

- MCU block including the configurable Interrupt/PEC controller and debug and break logic
- Configurable dual port RAM
- Configurable Interrupt/PEC controller
- All interfaces for system (on chip) integration, including X-Bus, PD peripheral bus, Local Memory bus (for ROM or SRAM).

The C166 architecture allows instruction execution and data access from all memory locations. This includes X-Bus, local memory bus, dual port and external memories.

All four bus Interfaces of the MCU (X-Bus, LM Bus, RAM Bus and PD Bus) are operated on at the same time by the MCU.

**TEAKLite:**

The TEAKLite core has 16-bit data and 16-bit program memory accesses, a high performance fixed-point DSP core, and low power consumption.

The core consists of a high performance processing unit including a full featured bit-manipulation unit, RAM and ROM addressing units, and program control logic. The core has an improved set of DSP and general microprocessor functions to meet application requirements. The programming model and instruction set are optimized for generation of efficient and compact code.

The Computation Unit consists of a 16 by 16 multiplier unit with a 32-bit product and a 36-bit ALU with two accumulator registers A0 and A1.

The Bit Manipulation Unit consists of a full 36-bit barrel shifter, an exponent unit, a bit-field operation unit, two 36-bit accumulator registers B0 and B1, and a shift value register.

The Data Address Arithmetic Unit performs all the address storage and address calculation necessary for accessing the data and program memories. It also supports a software stack pointer, loop counter, and min/max operations.

The key features of TEAKlite core are as follows:

- 16-bit fixed-point DSP core
- 16 x 16-bit 2's complement parallel multiplier with a 32-bit product
- Single cycle multiply-accumulate instructions
- 36-bit ALU
- 36-bit left/right barrel shifter
- Four 36-bit accumulators
- Software stack residing in the data RAM
- User-defined registers off-core
- Three high-active interrupt input lines INT0, INT1, and INT2
- Automatic context switching by interrupts
- Up to 16-bit Bit Field Operations (BFO)
- Three modes for power saving features: Operational, Idle, and Sleep.
- The maximum Frequency is 104 MHz. The TEAKlite core clock is scalable to lower frequencies.

**In the DSP Firmware are implemented the following functions:**

The High Speed Circuit Switched Data (HSCSD) class 4 is supported.
The packet-oriented data (GPRS) class 4 is supported with a coding schemes from 1 to 4. It provides fixed, dynamic and extended dynamic modes.

If the E-GOLDlite is used as a modem, the HSCSD and GPRS class 10 is supported. The packet-oriented data (GPRS) class 10 is supported with a coding schemes from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.

<u>Synchronisation and Measurements</u>

- Scanning of channels (measurement of the field strengths of neighboring base stations)
- Detection and evaluation of Frequency Correction Bursts.

<u>Equalization</u>

There is equalization of GMSK Normal Bursts and Synchronization Bursts with bit-by-bit soft output.

<u>Channel Coder/Decoder</u>

There are Channel Coders/Decoders for 2.4kbits/s, 4.8kbits/s, 9.6kbits/s, and 14.4kbits/s.

<u>Speech</u>

- A Speech Coder-Decoder: FR, EFR, AMR Narrow Band, or HR.
- Discontinuous transmission (DTX)
- Voice activity detection (VAD)
- Comfort noise generation (CNG).

<u>Voiceband</u>

- Generation of tones and side-tones
- Ringer tone generation
- Echo Cancellation (handsfree) with noise reduction

Also the functionality and the internal and external interfaces of the Audio Scheduler is implemented in DSP firmware of E-GOLDlite.

<u>Real Time Clock (integrated in the EGOLDlite):</u>
The real time clock (degree of accuracy 150ppm) is powered via a seperate voltage regulator inside the PMU. Via a capacitor, data is kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with which it is possible to switch the phone on and off.

## 6.3 SRAM

Memory for volatile data
Memory Size: 16 Mbit
Data Bus: 16Bit

## 6.4 FLASH

Memory Size: 128 Mbit (16Mbyte)
Data Bus: 16 Bit

## 6.5 SIM

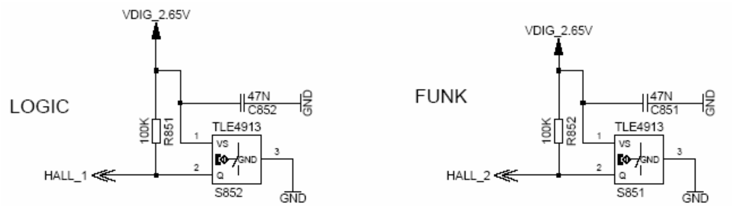
SIM cards with supply voltages of 1.8V and 3V are supported.

## 6.6 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts.

## 6.7 Magnetic Switch

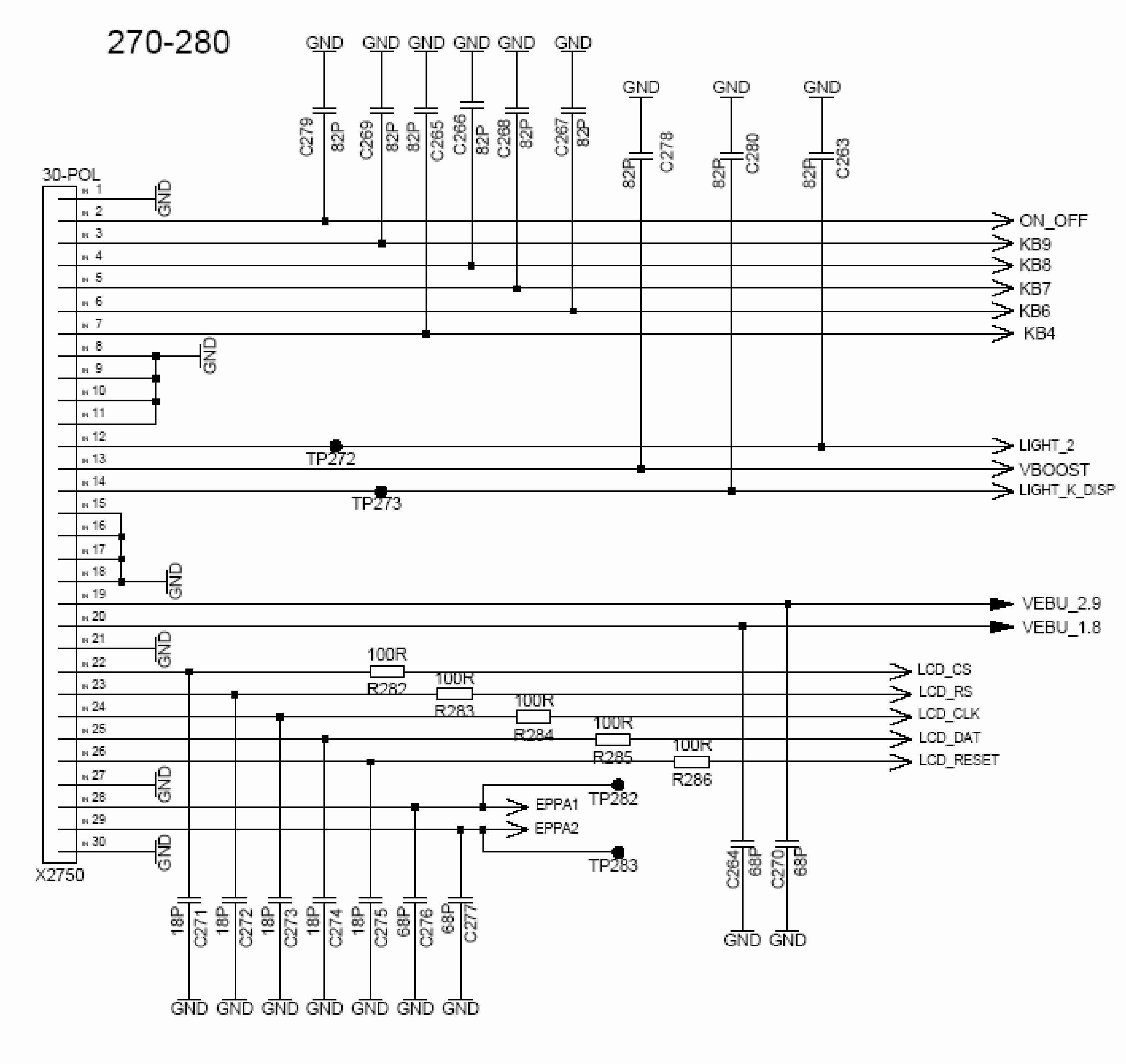
To identify the position of the slider, 2 Hall sensors (S852 lower position, S851 upper position) are placed on the PCB, 1 magnet is placed in the upper case.



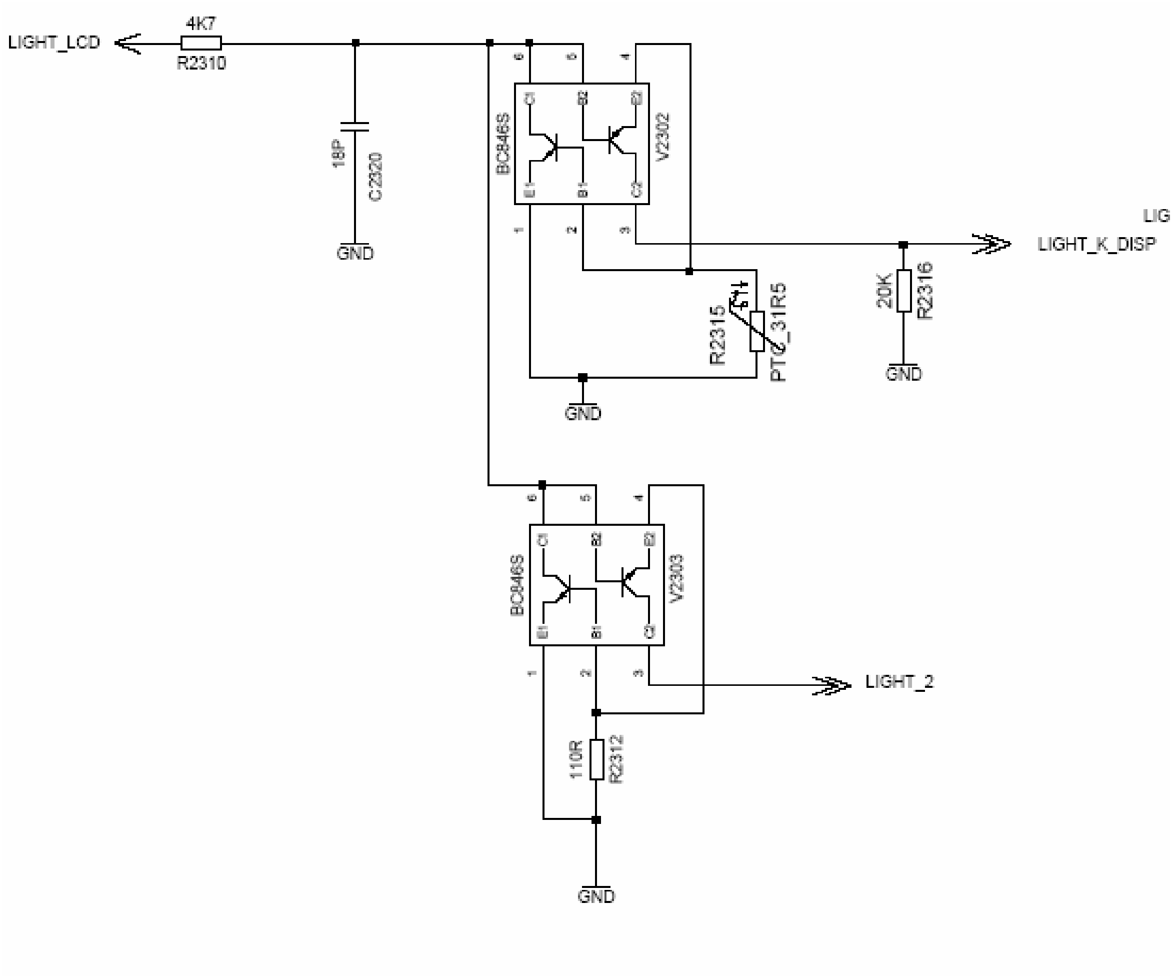
## 6.8 Display Modules

The CF110 display has a resolution of 130 x 130 square pixels with a color depth of 65k. It contains a active matrix panel where the colors are generated by color filter.
The controllers are directly mounted on the panel of the display. A small MMI board with components (keypad LEDs, resister) also include in the LCD module. LCD FPC & MMI FPC mounted on the MMI PCB by ACF.
The illumination for the Display is realized by 3 LEDs which can support write, blue and red.
All external components which are necessary to drive the controller for the Display are assembled on the LCD FPC. The interconnections to the Main-PCB include LCD I/F, MMI keypad I/F, Receiver I/F, and the power supply lines. The total module interface will be realized with a BtoB connector with 30 interconnections.

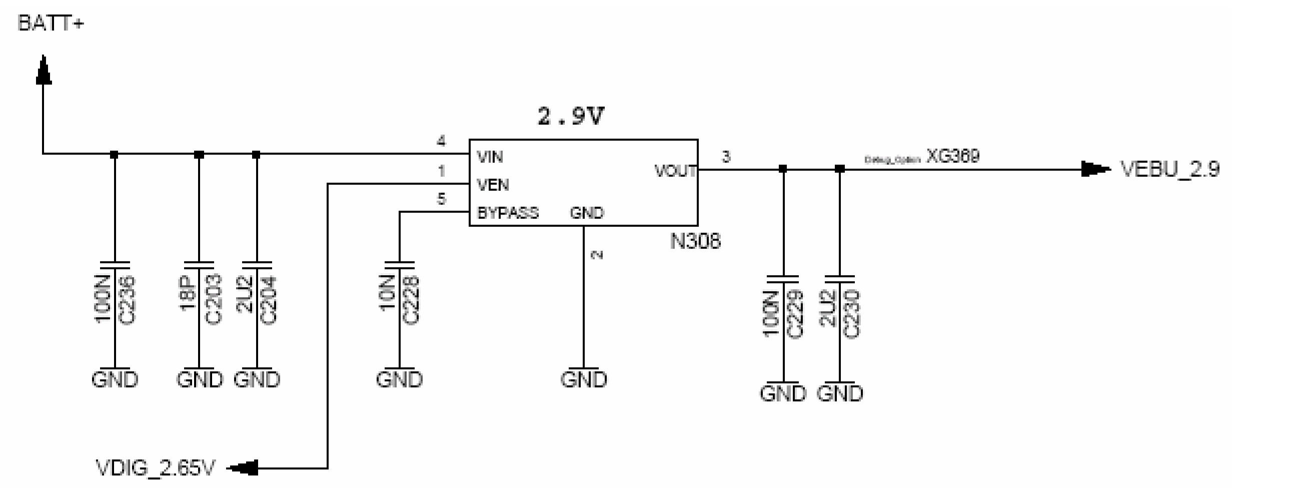
| Pin | Name | Remarks |
|---|---|---|
| 1 | GND | Ground |
| 2 | KB_ON_OFF | Keypad matrix |
| 3 | KB9 | Keypad matrix |
| 4 | KB8 | Keypad matrix |
| 5 | KB7 | Keypad matrix |
| 6 | KB6 | Keypad matrix |
| 7 | KB4 | Keypad matrix |
| 8 | GND | Ground |
| 9 | GND | Ground |
| 10 | GND | Ground |
| 11 | GND | Ground |
| 12 | LIGHT_2 | Cathode for Keypad LED |
| 13 | VBOOST | Anode LED for Display and Keypad LED |
| 14 | LIGHT_K_DISP | Cathode for Display LED |
| 15 | GND | Ground |
| 16 | GND | Ground |
| 17 | GND | Ground |
| 18 | GND | Ground |
| 19 | VEBU_2.9 | Power Supply for Display Interface I/O |
| 20 | VEBU_1.8 | Power Supply for Driver IC logic |
| 21 | GND | Ground |
| 22 | LCD_CS | Chip select, low active |
| 23 | LCD_RS | Register select, L = command H = data |
| 24 | LCD_CLK | Serial Clock |
| 25 | LCD_DAT | Serial Data |
| 26 | LCD_RESET | Reset, low active |
| 27 | GND | Ground |
| 28 | EPPA1 | Acoustic receiver |
| 29 | EPPA2 | Acoustic receiver |
| 30 | GND | Ground |


270-280
30-POL
X2750
ON_OFF
KB9
KB8
KB7
KB6
KB4
LIGHT_2
VBOOST
LIGHT_K_DISP
VEBU_2.9
VEBU_1.8
LCD_CS
LCD_RS
LCD_CLK
LCD_DAT
LCD_RESET
EPPA1
EPPA2
TP272
TP273
TP282
TP283
100R R282
100R R283
100R R284
100R R285
100R R286
C279 82P
C269 82P
C265 82P
C266 82P
C268 82P
C267 82P
C278 82P
C280 82P
C263 82P
C264 68P
C270 68P
C271 18P
C272 18P
C273 18P
C274 18P
C275 18P
C276 68P
C277 68P
GND

Required voltage for the display illumination is VBOOST.
With the signal LIGHT_LCD (P1) the illumination for the display is controlled.

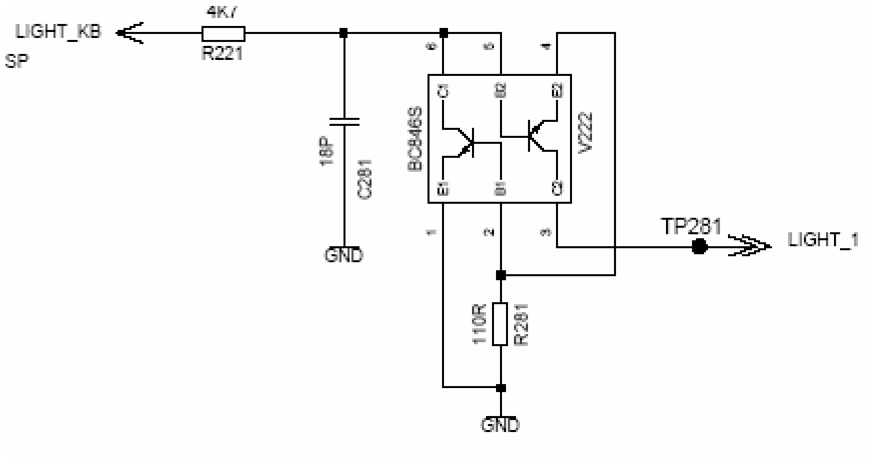


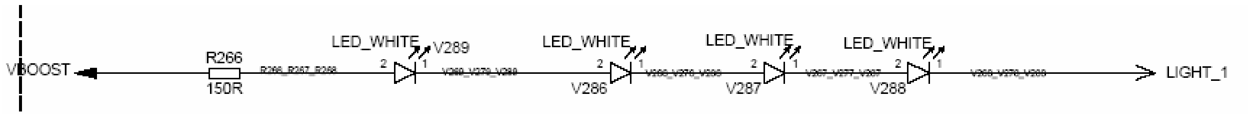

Required voltage for the display controller VEBU_2.9V.
The voltage regulator N308 with a nominal output voltage of 2.9V is used



## 6.9 Illumination – Keyboard

The LED´s are mounted on the upper side of the PCB. The illumination of the keypad will be done via high-brightness LEDs (colour: white, type: top-shooter, driven by 6 mA / LED). The light is switched via switches inside the EGOLDlite. With the signal LIGHT_KB (R5) the illumination for the keyboard is controlled.



# 7 Acoustic

The speaker module is designed to provide good performance for mobile handsfree and sound ringer. The speaker module is based on X75G speaker core with a closed back volume. It is mounted below antenna carrier. The antenna carrier builds a channel on the speaker module, the sound goes through this channel to the left and right sides of the phone, where there are sound outlet holes. The speaker module contacts to the PCB by 2 coil springs. There are two impeders connected on the lead wires of speaker, it's solution for the impact to RF. In ringer mode acoustic shock is avoided by using ramping of the ringer level. The speaker is driven by the MONO output in PMU.

A rectangular type receiver is used for voice, which can reduce the length of the phone. It is in the slider part. The receiver has a plastic case for sealing an individual volume, so the performance of receiver won't be affected when slider parts goes up or down. The tube in the case is connected to the top of the phone. It can improve the low frequency response in handset mode. The receiver is driven by the Egold Lite.

The microphone is built in the base part lower case. It's a 4mm omni directional microphone, contacting on the main PCB by coil springs.

The microphone is combined with a plastic boot, the sealing is provided by a double adhesive tape on the front of microphone.

The buzzer and the keypad clicks will be realized over the speaker.
The standard sounds will be generated by the EGOLDlite, the advanced sounds will be generated via firmware running on the DSP.

# 8 Power Supply, Battery and Charging

All the important functions for the power supply of the phone are carried out by the power supply ASIC.
The POWER-pin of the I/O-Connector is for charging the battery with an external power supply.

## 8.1 Power Supply ASIC

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- Voltage regulator
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I2C interface)
- Bandgap reference
- Audio multiplexer
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I2S Interface

**Power Supply Operating modes:**

The ASIC can be used in different operating modes:

| Mode | Pin Requirements | Description |
|---|---|---|
| Power down mode with minimum activity | ON/OFF<br>ON/OFF2<br>VDD_CHARGE | In power down mode the current consumption of the ASIC is very low. The inputs for switch on conditions (Pin ON/OFF, ON/OFF2,VDD_CHARGE), the LPREG, Bandgap reference, and the POR cells are active. All other blocks are switched off, so the battery is not discharged. This state is called “phone off. |
| Start Up Mode | ON_OFF<br>ON_OFF2 | Start Up Mode can be initiated by ON_OFF or ON_OFF2. In this mode a sequential start-up of references (this includes the reference buffer and the biasing cell), oscillator., voltage supervision and regulators is controlled by digital part. In failure case (undervoltage, overvoltage or time out of the µC reaction)., the ASIC is shut down. |
| Full operating mode | VDD_CHARGE<br>CHARGE_UC | All blocks are active. Trickle charge is switched off. The blocks fast charge and charge monitor can be active only in this mode. These modes will be activated with VDD_CHARGE or CHARGE_UC. The name of this mode is “phone on” or “active mode”. The border between the startup phase and the active mode is the rising edge of the RESETN signal. This will allow the uC to start working. |

| Mode | Pin Requirements | Description |
|---|---|---|
| Active Mode (submode of Full operating mode) | | In this mode, the uC controls the charging block and most of the failure cases. The ASIC can be controlled by the TWI interface, interrupts can be sent by the ASIC. Further, the temperature and the voltages are supervised (in case of failure, the uC will be informed). In case of watchdog failure, overvoltage or power on reset, the ASIC will be switched off immediately. The mono and stereo audio block can be switched on in active mode. |
| Sleep Mode with special low current operating mode for the LDOs (submode of Full operating mode) | SLEEP1_N<br>TC_ON<br>CHARGE_uC | A low level at the pin SLEEP1_N will switch the phone from the mode “PHONE ON” to sleep mode. This mode can be activated out of the active mode. In sleep mode trickle charge (TC_ON), fast charge (CHARGE_UC), supply overvoltage detection, supply undervoltage detection, audio function are switched off. LDO undervoltage detection, clock and all reference voltages are active. LDOs are working in low current mode. The possibility to supply the ASIC from VDD_CHARGE with the internal LDO is switched off. Only the battery can be used for supply. This mode is called “phone stand-by”. |
| Trickle charge mode to be able to support charging of the battery | VDD_CHARGE<br>EXT_PWR | In case of a rising edge at VDD_CHARGE the ASIC goes from power down to interim mode. In this mode, the oscillator and the reference are started. The fuses are read in. If the voltage is high enough (after a delay time of 1 ms to filter a ringing), the signal EXT_PWR is going to H and the power up continues. The ASIC shuts off if the voltage is below threshold. In Trickle Charge Mode, first the charge unit starts and charges the battery in case of undervoltage. After reaching this threshold voltage or if the battery has enough voltage from the beginning, a start up similar to the regular startup mode is initiated. In case of voltage drop under battery threshold, the first trickle charging can be started again until the Active Mode is entered. In this case, the internal VDDREF regulator, the reference generator and oscillator are started and the ASIC is supplied by VDDREF. If any failure is detected, the ASIC is switched off. |

## Power Supply Functions:

| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Switching on the mobile phone | ON_OFF,<br>ON_OFF2,<br>VDD_CHARGE | There are 3 different possibilities to switch on the phone by external pins:<br>- VDD_CHARGE with rising edge after POR or high level at end of POR signal<br>- ON/OFF with falling edge<br>- ON/OFF2 with rising edge<br>In order to guarantee a defined start-up behaviour of the external components, a sequential power up is used and the correct start up of these blocks is supervised. In active mode, a continuous signal at watchdog is needed to keep the system running. If the signals fails, the ASIC will switch to power down mode. It must be guaranteed that each start-up condition does not interfere and block the other possible startup signals. In case of failure during start-up, the device will go back to power down mode. To guarantee that VDDCHARGE is always sensed we must be able to detect whether the VDDCHARGE will have a rising edge during POR (this can happen in case of an empty battery). Therefore this signal is sensed as level sensitive at the end of POR and edge sensitive after POR signal. |
| Watchdog monitoring | WDOG | As soon as the first WDOG pin rising is detected during the TE4 timer, the device start the watchdog monitoring procedure. Standard switch off of the phone is the watchdog. The first edge of watchdog is rising. If a falling edge is detected as the first transient the device will go to power down mode again and the whole phone is switched off. Rising and falling edges must be detected alternated. With any edge on WDOG pin a counter will be loaded. The next - compared to the previous edge - inverted edge must occur between end of T1, and end of T2. If the signal occurs before end of T1 or is not detected until end of T2, the device will go to power down mode immediately after the violation of the watchdog criteria occurs.<br>T1 min. 0,327s/ typ. 0,360s/ max. 0,400s<br>T2 min. 2,600s/ typ. 2,860s/ max. 3,178s |
| Power-On-Reset (POR) | RESET_N<br>RESET2_N | To guarantee a correct start-up of the ASIC, a power on reset is needed at first power supply ramping. Therefore a static/dynamic power on reset circuit is added, which creates a reset each time the power supply is connected. After POR the ASIC starts up the reference and the oscillator, read in the fuse content and goes back to power down mode. If the power supply will drop under the POR threshold $V_{th,POR\_L}$ a synchronous reset is done and the ASIC will go to power down mode independently of the previous operating mode.<br>$V_{th,POR\_L}$ = min. 2.38/ typ. 2.43/ max. 2.48V |

| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Voltage Supply Logics | REG1 (2.65V) | The linear controller is designed for 2.65V(±2%) and a maximum load current of 140 mA.<br>Voltage and current for the external Logic is supplied from the internal 2.65V logic regulator. The operating voltage VREG1 is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference |
| Voltage Supply Logics | REG2 (1,5V) | The linear controller is designed for 1.5V (±2%) and a maximum load current of 300 mA.<br>The output voltage can be adjusted to four different values with TWI register by the µC. The selectable values are 1.5(default), 1.82, 1.92 and 2.0V.<br>The REG2 supplies the Baseband Processor. |
| Voltage Supply Logics | REG3 (2.65V) | The linear controller is designed for 2.65V(±3%) and a maximum load current of 140 mA.<br>It will consist basically of an internal operation amplifier, an integrated p-channel output transistor as well as a capacitor (C = 2.2µF) for stabilising the voltage. The required reference voltage for the regulating circuit will be generated internally via a band gap. The negative feedback of the regulating circuit shall be done via chip-internal resistances. |
| Voltage Supply RF | VREGRF1, SLEEP1_N, SLEEP2_N, POWER_ON | The linear controller is designed for 2.755V (±2%) and a maximum load current of 150 mA. The output voltage can be adjusted to three different values with TWI register by the µC. The selectable values are 2.755V(default), 2.54V, and 2.85V.<br>Voltage and current for RF-VCO and Transceiver is supplied from the internal 2.755V LDO. The operating voltage RF1LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed.<br>RF1LDO is controlled by SLEEP1_N and SLEEP2_N. If one of them is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF1LDO can only be enabled by TWI bit. In external mode, RF1LDO can only be enabled by SLEEP1_N or SLEEP2_N.<br>RF1LDO is released with rising edge of POWER_ON signal. |
| Voltage Supply RF | VREGRF2, RF_EN, RESET_N | The linear controller is designed for 1.53V (±2%) and a maximum load current of 180 mA. The output voltage can be adjusted to three different values with TWI register by the µC. The selectable values are 1.53V(default), 2.70V, and 2.85V.<br>Voltage and current for RF-VCO and Transceiver is supplied from the internal 1.53V LDO. The operating voltage RF2LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed.<br>RF2LDO is controlled by RF_EN. If it is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF2LDO can only be enabled by TWI bit. In external mode, RF2LDO can only be enabled by RF_EN.<br>RF2LDO is released with rising edge of RESET_N signal. |

| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Voltage Supply Audio | VREGA | The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 190 mA.<br>VDDA is used for the whole stereo analog supply. The DAC digital (VDDDAC), Low Noise Bandgap, Mono- and Stereoamplifier supplies are connected to VREGA or VBAT or an external LDO at 2.9V +/-5%. The AUDIO performances are guaranteed only, if the VREGA supplies all the stereo path.<br>VREGA is controlled with TWI registers directly by the µC. |
| Voltage Supply RTC | VLPREG | The linear controller is designed for 2.00V(min. 1.9V, max. 2.1V) and a maximum load current of 1 mA.<br>The output voltage can be adjusted to four different values with TWI register by the µC. The selectable values are 2.00(default), 1.82, 1.92 and 2.07V. LP-LDO is always working and will switch of only with POR signal. |
| Voltage Supply SIM | VREGSIM | The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 60 mA. The output voltage can be adjusted to a different value with TWI register by the µC to 1.8V(min. 1.76V, max. 1.84V).<br>This regulator can be activated by TWI register, but only in active mode. If the regulator is in power down, the output is pulled down by a transistor to avoid electrostatic charging of VREGSIM. |
| Charge Support | CHARGE_UC, CHARGE, VDDCHARGE, AVDD, SENSE_IN, TBAT | A charge support will be integrated for controlling the battery charge function. It consists basically of a temperature sensor, an external charge FET, an integrated High-side driver for the external FET with an external resistor between the source and the gate of the charge FET.<br>In the case of a rising edge at the CHARGE_UP the power source will be switched on. In this way the charge FET becomes conducting, provided that the integrated temperature comparator does not give the signal for extreme temperature and that no overvoltage is present at the VDD. In the case of falling slope at the CHARGE_UP, the current source is switched off and the pull-up resistor will make sure that the charge FET is blocked after a finite time.<br>Temperature switchoff becomes effective at approx. T>60°C. |
| Voltage supervision | | The levels of regulator REG1, REG2, REGA, SIM_LDO, and also the supply voltage VBAT are supervised with comparators. |
| Supervision of REG1 and REG2 | REG1<br>REG2 | In active mode the regulators are supervised permanently. If the voltage is under the threshold, the pin RESET_N stay Low and the ASIC go back to the power down mode. If the voltage is longer than Tmin under threshold voltage, the RESET_N is going to Low (Missing Watchdog signal -> phone switched off). The level of regulator REG1 and REG2 will be supervised permanently. If the voltage doesn't reach the threshold value at switch on, the RESET_N pin will stay low and the ASIC will go back to power down mode. The voltages are sensed continuously and digitally filtered with a time constant Tmin. If the regulator voltage is under threshold longer than Tmin, the RESET_N signal change to low and the uC will go to RESET condition (Missing Watchdog signal -> phone switched off). |

| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Powersupply supervision | VDD | If the battery voltage VDD exceeds VDD_high everything is switched off immediately within 1µs. Only the pullup circuitry for the external charge PMOS are active and will discharge the gate of the external PMOS |
| VDDA supervision | VDDA | To provide a short circuit protection at output of VDDA and output of stereo buffer a voltage supervision is implemented. If the VDDA output is less then this threshold, the VDDA will be switched off for 128ms. After this time the VDDA will be started again. The VDDA supervision starts 60ms after startup of VDDA. |
| Battery temperature supervision | | Charging is stopped, when overtemperatur occurs. Within 128ms, 3 values are measured. When these 3 values are identical status can be changed. The supervision is active in fast charge or trickle charge mode. Voltage on pin TBAT becomes smaller when temperature increases. If Vbat < (Vref_exe - Vhyst) charging is disabled. Only when Vtbatt > Vref_exe charging is enabled again. |
| Device temperature supervision | | To protect the ASIC, the temperature is supervised. The temperature is polled every 128ms and is filtered as in battery temperature supervision. If overtemperatur is detected, a bit in the STATUS register is set and an interrupt is generated. Monitoring is started only in active mode. |
| Analog switch Outport | | The level can be defined by the bit out_port_high of the TWI register. The high level can be derived of VREG2 or VREG3. Additional a pulldown transistor is connected to this node. |
| TWI Interface | TWI_CLK,<br>TWI_DATA,<br>TWI_INT | The TWI interface is an I2C compatible 2-wire interface with an additional interrrupt pin to inform the µC about special conditions.<br>The interface can handele clock rates up to 400 kHz. The device adress is 010001B (31H) |
| Audio mode functions | | Four audio amplifiers are integrated to support these modes:<br>1. Supply the speaker in the phone with audio signals including the possibility of handsfree and antipop switch on and off. This is the AUDIO MONO MODE.<br>2. Supply the speaker in the phone with ringing signal (RINGER MODE)<br>3. Transfer a key click, generated in digital part to the speaker. (KEY-CLICK FUNCTION)<br>4. Supply of stereo head set with stereo signal with short circuit protection. This is called the AUDIO STEREO MODE. These different modes with gain and multiplexing can be controlled via TWI. Also the output can be switched to TRI-STATE via TWI interface. |

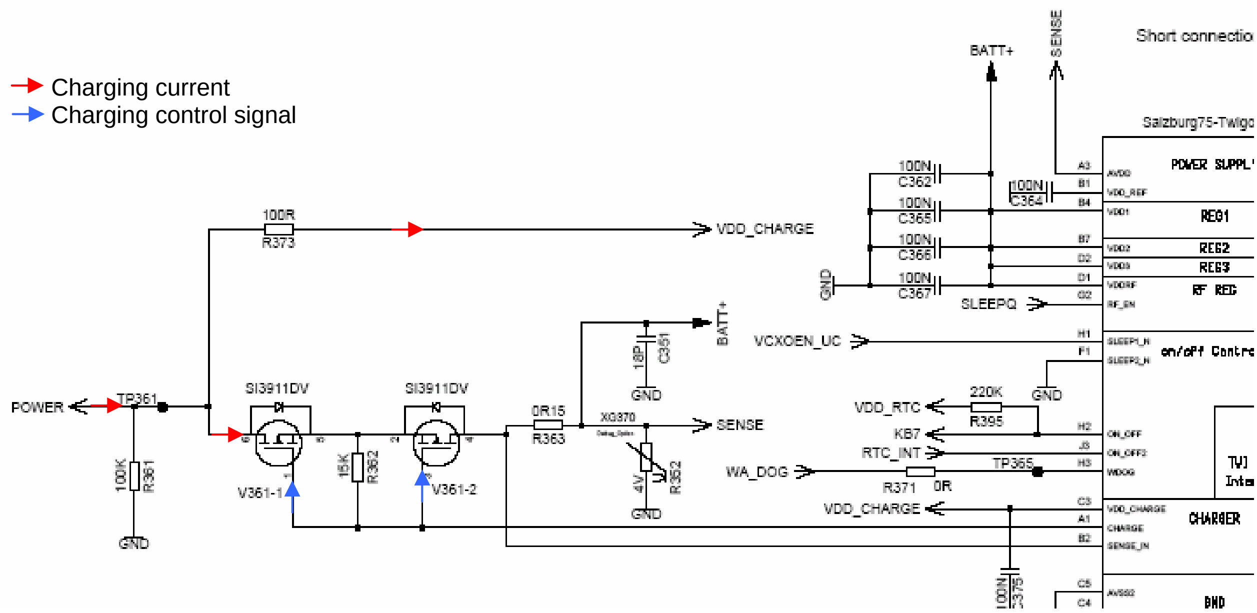
| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Audio Mono Mode | VREGA<br>MONO1<br>MONO2<br>VREFEX_M | This mode is the main function of the amplifier. The two amplifiers are used as differential mono amplifier to drive the speaker in the phone as external load. This differential approach allows delivering an optimum of power to the speaker, also in low voltage mode. Both amplifier paths are inverting amplifiers with external AC coupling at the input to compensate offset failures. The gain can be adjusted with the TWI interface. The output stage of the amplifiers must be able to drive a low impedance load as a external speaker for the handsfree application.<br>General parameters: Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB. The signals for the amplifier are connected via an audio multiplexer with 3 pairs of input signals. |
| Audio Stereo Mode | VDDSTEREO<br>STEREO1<br>STEREO2<br>STEREOM | For stereo mode 2 single ended buffers are used. These buffers will be supplied by the additional regulator with 2.9 Volt to be more stable against the GSM ripple on the battery voltage. Also reference voltage for the buffers is generated by a high precision, low noise bandgap reference for better performance. An external capacitor is needed to filter this reference additionally. The gain steps for the programmable gain amplifier are identical with the mono amplifier. Nokeyclick and ringer needed for the stero part. Gain can be controlled with the TWI. The connected speaker has an impedance of typical 16 Ohm. To guarantee a ANTI-POP noise a digital startup is implemented. This will allow a soft start of the VMID and creates a “clean” audio band during the startup. For eliminating external coupling capacitors for the speaker, an additional amplifier creates virtual ground (for both speakers). Accordingly to this, the max current of the virtual ground has to be the double of the normal output amplifier. Due to the power amplifier offset a DC current appear in the headset. Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB |
| Ringer function | RINGIN | In ringer mode the ringing signal is transferred via the amplifier to the speaker to eliminate the additional buzzer. The speaker is controlled with a rectangular signal RINGIN. Input signal is digital signal with variable frequency. Amplitude is adjusted by TWI register.<br>For start-up a smaller time constant must be used to allow a fast switch on behaviour. Ringing function can be started at any time. If the audio is off, the start-up is done with RINGER time constant. If audio is starting with AUDIO start-up, the time constant is switched to RINGER mode, too. If the audio amplifier is already up and running, the RINGIN is connected to the amplifier and audio sigal is muted due to open multiplexer. |

| Functions | Pin Requirements | Implementation/Sequence |
|---|---|---|
| Key click function | | Pushing a key of the phone can be combined with a key click. This function is also realized with the audio amplifier in pulsed mode. The ASIC creates a digital PWM signal. Frequency of the PWM signal is 3.5 kHz.<br>The start-up is similar to the ringer function. If the audio is off, the start-up is done with KEYCLICK time constant. If audio is starting with AUDIO start-up, the time constant is switched to KEYCLICK mode, too. If the audio amplifier is already up and running, the KEYCLICK is connected to the amplifier and audio sigal is muted due to open multiplexer. |
| Audio Multiplex Matrix | AUDIOA1<br>AUDIOA2<br>AUDIOB1<br>AUDIOB2<br>AUDIOC1<br>AUDIOC2 | Each of the three input sources should be switched to Mono and Stereo outputs. Furthermore a conversion can be done. Following sources:<br>- Mono differential<br>- Mono Single Ended (both channels parallel)<br>- Stereo<br>The DAC can be switched off for using the analog external inputs. This principle will allow to do each combination and have different modes for stereo and mono in parallel. |
| I2S Interface | CLO,<br>WAO,<br>DAO | The I2S Interface is a three wire connection that handels two timemultiplexed data channels. The three lines are the clock (CLO), the serial data line (DAO) and the word select line (WAO). The master I2S also generates the appropriate clock frequncy for CLO set to 32 times the sampling rate (FS) |
| Audio DAC | VDDDAC | For digital to analog conversion a 16 bit sigma delta converter is used. Digital input signal is delivered with a I2S interface. The I2S interface should be 16 bit format. To be able to work with allpossible operating modes, the sampling frequency can vary from 8kHz to 48kHz. The performance of the audio output signal must be guaranteed over the full range the human ear is able to hear. This means for FS=8kHz the noise at frequencies higher than FS/2 must be suppressed. This is done by DSP in a single ended 2$^{nd}$ order Low Pass filter. The clock for the I2S will be varied accordingly to the sampling frequency. Therefore a clock recovery based on CLO signal of the I2S can be implemented. This clock recovery must smooth any jitter of this clock to reduce the noise of the DAC. |
| PLL | VDDPLL<br>PLLOUT | The PLL will have three frequency modes to produce a 32xCLO clock for the DSP and the DAC. The loop filter is realised with an external RC circuit. This PLL also contains a lock detector circuit. |

## 8.2 Battery

As a standard battery a LiIon battery with a nominal capacity of 3,7 Volt/700mAh is used.

## 8.3 Charging Concept




### 8.3.1.1 Charging Concept

**General**

The battery is charged in the unit itself. The hardware and software is designed for LiIon with 4.2V technology.

Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging takes place in the background (the customer can see this via the “Charge” symbol in the display). During normal use the phone is being charged (restrictions: see below).

Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The EGOLDlite takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the POWER SUPPLY ASIC hardware can override/interrupt the charging in the case of over voltage of the battery (only for Manganese Chemistry Battery types e.g. NEC).

With the new slim Lumberg IO connector we lose the charger recognition via SB line. Now we measure the charge current inside the POWER SUPPLY ASIC with a current monitor.

The charging software is able to charge the battery with an input current within the range of 350-600mA. If the Charge-Fet is switched off, then no charging current will flow into the battery (exception is trickle charging, see below).

For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. The NTC for the ambient temperature will be on the PCB (26 MHz part).

**Measurement of Battery, Battery Type and Ambient Temperature**

For the conversion of signals like battery voltage, battery type, temperature, EGOLDlite provides identical measurement interfaces. Measurement circuit is consisting of external sensing components and integrated analog multiplexers and switches. Through corresponding switch settings, the measured signal is passed to input of ADC. 12-bit conversion results are readout by µc and used for charging control.

**Charging Characteristic of Lithium-Ion Cells**

LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is approx. 600mA, minimum about 100mA. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be started ranges from 5...40°C, and the temperature at which charging takes place is from 0...45°C. Outside this range no charging takes place, the battery only supplies current.

**Trickle Charging**

The POWER SUPPLY ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the POWER SUPPLY ASIC. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.75V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the POWER SUPPLY ASIC will switch on the phone automatically and normal charging will be initiated by software (note the restrictions on this item as stated below).

**Normal Charging**

For battery voltages above 3.2 Volt and normal ambient temperature between 5 and 40°C the battery can be charged with a charge current up to 1C*. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the POWER SUPPLY ASIC. The level of charge current is limited/controlled by the accessory or charger.

**Restrictions**

A battery which has completely run down can not be re-charged quickly because the battery voltage is less than 3.0V and the logic which implements the charge control cannot be operated at this low voltage level. In this case the battery is recharged via trickle-charging. However, the charging symbol cannot be shown in the display because at this time logic supply voltages are not operating. The charging time for this trickle-charging (until the battery can be fast-charged from then on) is in the range of 1 hour. If, within this time, the battery voltage exceeds 3.2V, then the PMU switches on the mobile and charging continues in the Charge-Only Mode. In some circumstances it can happen that after trickle-charging and the usually initiated switch-on procedure of the mobile, the supply voltage collapses so much that the mobile phone switches off again. In this case trickle charging starts again with a now raised threshold voltage of 3.75V instead of 3.2V, at maximum for 20 minutes. The PMU will retry switching on the phone up to 3 times (within 60 minutes overall).

Charging the battery will not be fully supported in case of using old accessory (generation '45' or earlier). It is not recommended to use any cables that adapt "old" to "new" Lumberg connector. Using such adapters with Marlin will have at least the following impact:

half-sine wave chargers (e.g. P35 & home station) can not be used for trickle charging

normal charging might be aborted before the battery is fully charged

EMC compliance can not be guaranteed

A phone with a fully charged LiIon battery will not be charged immediately after switch-on. Any input current would cause an increase of the battery voltage above the maximum permissible value. As soon as the battery has been discharged to a level of about 95% (due to current consumption while use), it will be re-charged in normal charging mode.

The phone cannot be operated without a battery.

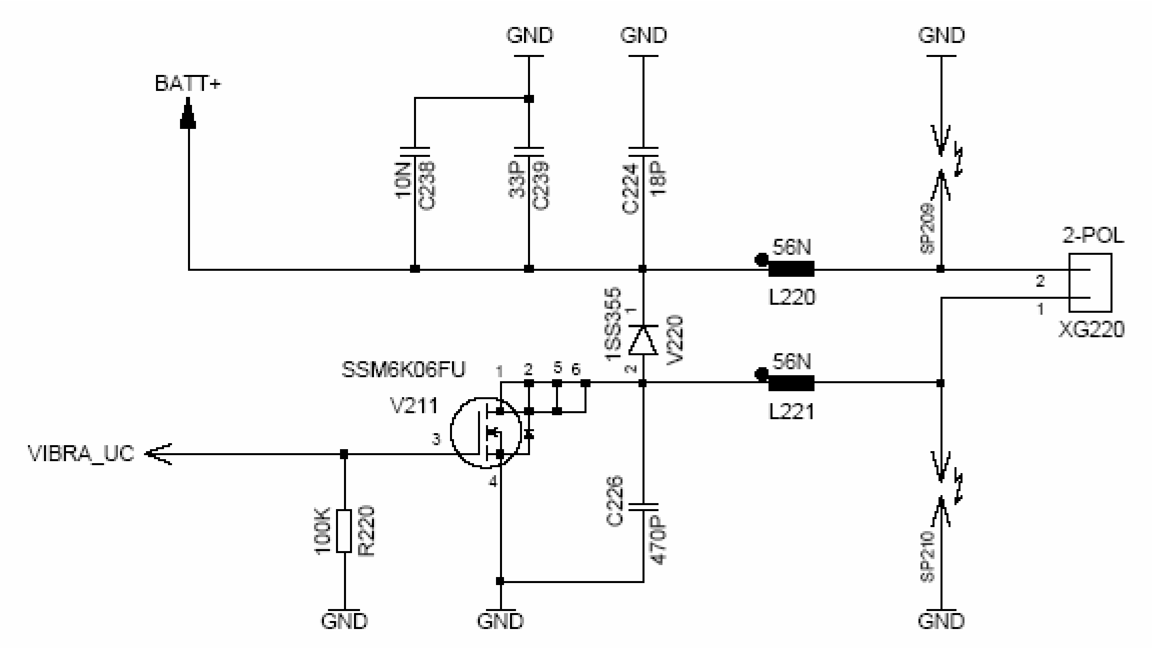
The phone will be destroyed if the battery is inserted with reversed polarity.

The mobile phone might be destroyed by connecting an unsuitable charger.

In case the transistor fails the ASIC will be destroyed. In the case of voltages lower than 15V and an improper current limitation the battery might be permanently damaged. A protection against grossly negligent use by the customer (e.g. direct connection of the charge contact to the electricity supply in a motor car) is not provided. Customer safety will not be affected by this restriction.

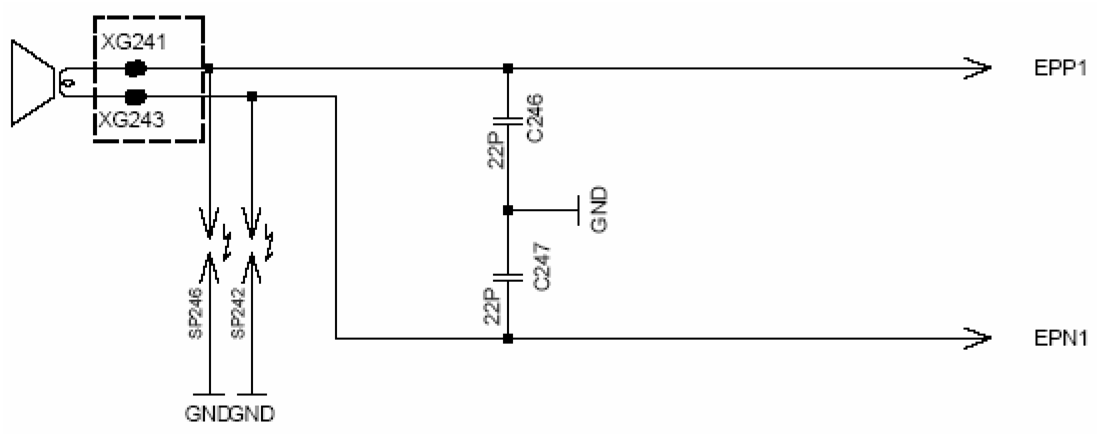
# Interfaces

## 8.4 Vibra (XG220)



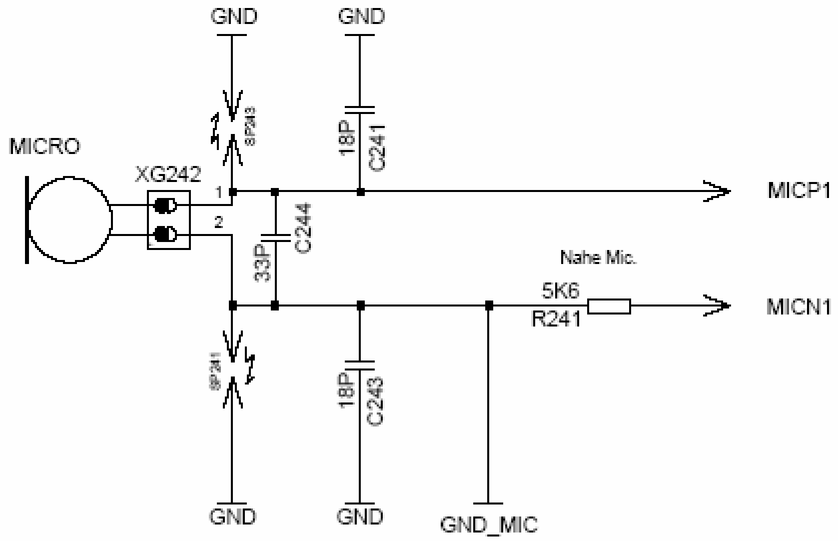

| Pin | IN/OUT | Remarks |
|---|---|---|
| 1 | I | The FET V211, switching this signal, is controlled via the EGOLDLite signal VIBRA_UC. |
| 2 | O | BATT+ |

## 8.5 Earpiece (XG243)



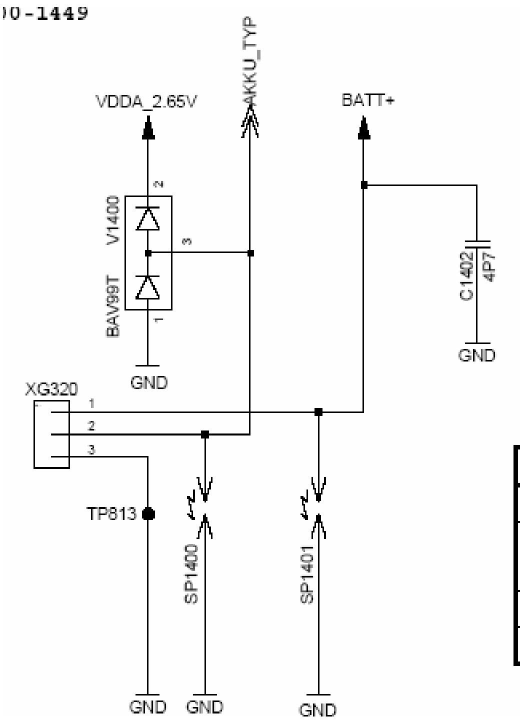

| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 1 | EPP1 | O | 1st connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. EPP1 builds together with EPN1 the differential output to drive the multifunctional "earpiece" (earpiece, ringer, handsfree function). |
| 2 | EPN1 | O | 2nd connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. |

## 8.6 Microphone




| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 1 | MICP1 | O | Microphone power supply. The same line carries the frequency speech signal. |
| 2 | GND_MIC | | |

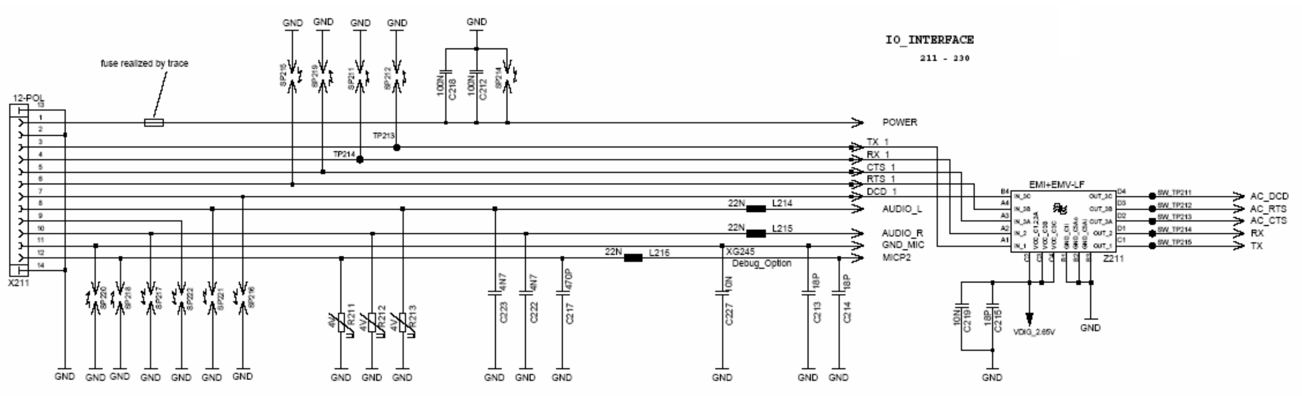
## 8.7 Battery (X181)




| Pin | Name | Level | Remarks |
|---|---|---|---|
| 1 | BATT+ | 3 V... 4.5V | Positive battery pole |
| 2 | AKKU_TYP | 0V...2.65V | Recognition of battery/supplier |
| 3 | GND | - | Ground |
| 4 | GND | - | Ground |

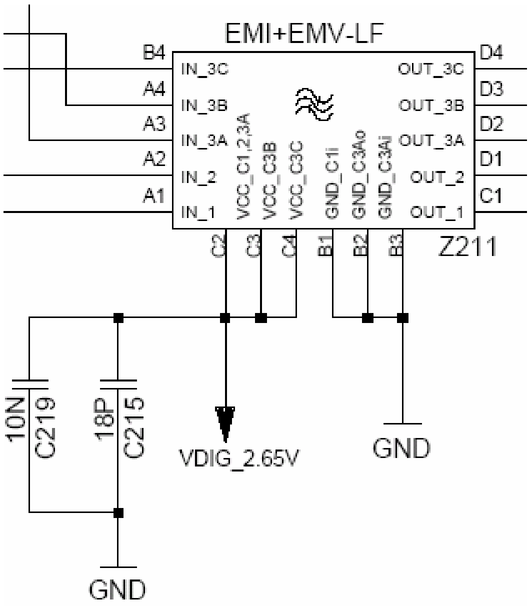
## 8.8 IO Connector (X211) with ESD protection (Z211)

### IO Connector



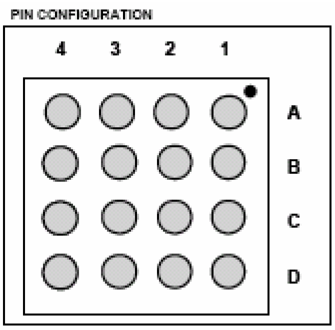

| Pin | Name | IN/OUT | Notes |
|---|---|---|---|
| 1 | POWER | I/O | POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories. |
| 2 | GND | | |
| 3 | TX | O | Serial interface |
| 4 | RX | I | Serial interface |
| 5 | DATA/CTS | I/O | Data-line for accessory-bus<br>Use as CTS in data operation. |
| 6 | RTS | I/O | Use as RTS in data-operation. |
| 7 | CLK/DCD | I/O | Clock-line for accessory-bus.<br>Use as DTC in data-operation. |
| 8 | AUDIO_L | Analog O | driving ext. left speaker<br>With mono-headset Audio_L and Audio_R differential mode |
| 9 | GND | | |
| 10 | AUDIO_R | Analog O | driving ext. right speaker With mono-headset Audio_L and Audio_R differential Signal |
| 11 | GND_MIC | Analog I | for ext. microphone |
| 12 | MICP2 | Analog I | External microphone |

## ESD Protection with EMI filter




The Z211 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z211 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages up to 8 kV.

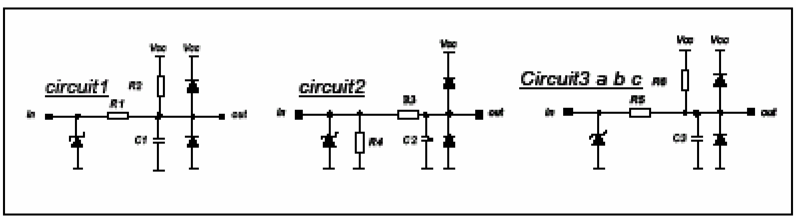
Pin configuration of the Z211



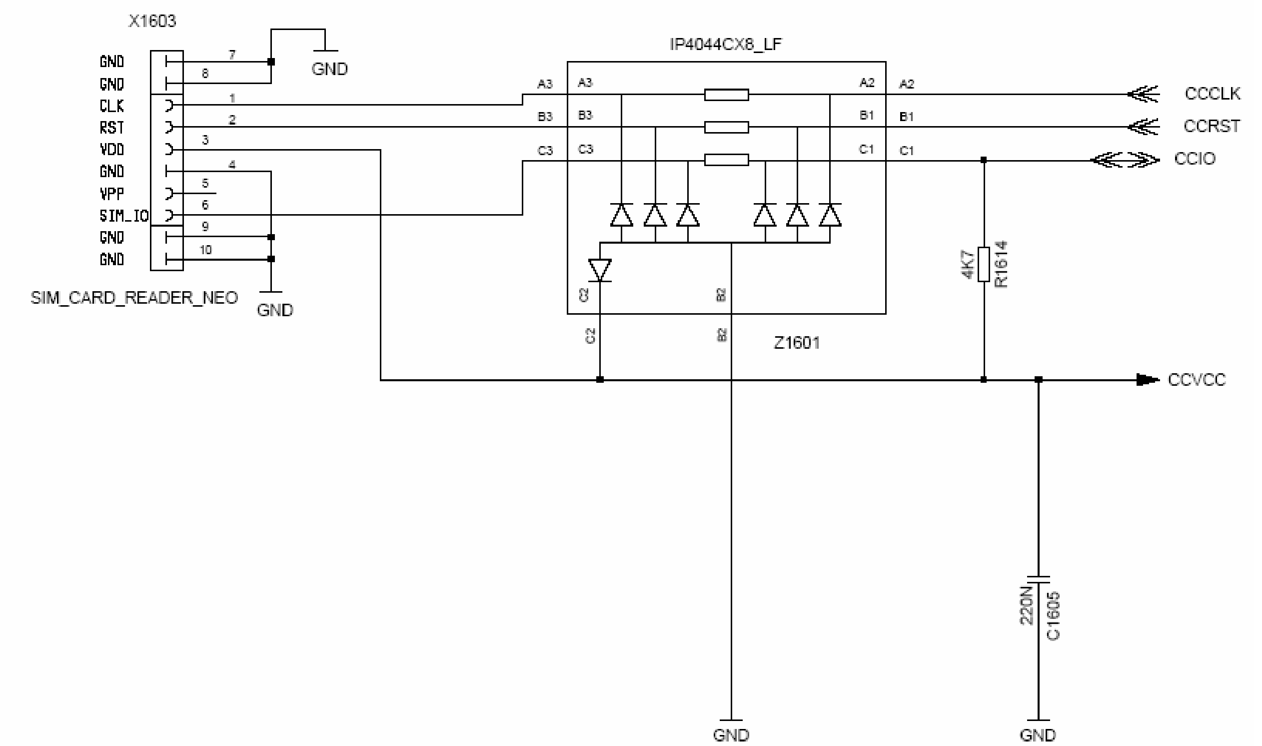

| | | | |
|---|---|---|---|
| A1 | Input C1 | C1 | Output C1 |
| A2 | Input C2 | C2 | Vcc C1 / C2 / C3A |
| A3 | Input C3A | C3 | Vcc C3B |
| A4 | Input C3B | C4 | Vcc C3C |
| B1 | GND C1I / C1o / C2o | D1 | Output C2 |
| B2 | GND C3Ao / C2I | D2 | Output C3A |
| B3 | GND C3AI / C3BI / C3Bo / C3CI / C3Co | D3 | Output C3B |
| B4 | Input C3C | D4 | Output C3C |

Z211 Circuit Configuration

Circuit configuration



## 8.9 SIM




| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 1 | CCLK | O | Pulse for chipcard.<br>The chipcard is controlled directly from the EGOLDlite. |
| 2 | CCRST | O | Reset for chipcard |
| 6 | CCIO | I | Data pin for chipcard; |
| | | O | 10 kΩ pull up at the CCVCC pin |
| 3 | CCVCC | - | Switchable power supply for chipcard;<br>220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes. |

# 9 Keyboard

The keyboard is connected via the lines KB0 – KB9 with the EGOLDlite.
KB 7 is used for the ON/OFF switch. The lines KB0 – KB5 are used as output signals. In the matrix KB6, KB8 and KB9 are used as input signals for the EGOLDlite.