Service Repair Documentation
Level 2.5e – IFX
C65, C70, CX70, C72

Release	Date	Department	Notes to change
R 1.0	23.03.2006	BenQ S CC CES	New document

Table of Contents:

1 List of available level 3 parts C65IFX

Product	ID	Order Number	Description CM
C65	C1000	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1123	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1200	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1201	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1202	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1203	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1204	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1205	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1206	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1207	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1208	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1209	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1211	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1302	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1303	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1304	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1308	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1309	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1310	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1311	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1312	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1313	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1314	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1315	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1317	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1318	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1319	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1329	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1330	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1331	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1332	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C65	C1355	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
C65	C1356	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
C65	C1381	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C1382	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C2232	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)

C65	C3600	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3601	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3602	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3603	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3610	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3621	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C3988	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C4001	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	C4040	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C65	D1000	L36810-G6191-D670	IC SGOLDLITE PMB8875 V1X
C65	D1300	L36145-J4683-Y19	IC ASIC D1094DA MOZART/TWIGO4
C65	D3601	L36820-U6054-D670	IC CAMERA INTERFACE S1D13716B02
C65	D4001	L50610-L6111-D670	IC TRANCEIVER PMB6270 SMARTI SD
C65	D4031	L50645-K280-Y277	IC FEM EPCOS 900 1800 1900MHZ (Fem-Type4)
C65	L1300	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C65	L1301	L36151-F5103-M3	COIL 10U (Co-Type1)
C65	L1302	L36151-F5472-M1	COIL 4U7 (Co-Type3)
C65	L1318	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C65	L1331	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C65	N1501	L36810-B6132-D670	IC LOGIC DUAL BUS SWITCH US8
C65	N3600	L36810-C6134-D670	IC V-REG 2.9V (Vr-Type1)
C65	N3981	L50651-Z2002-A78	IC MODUL PA PF0814 (PA-Type2)
C65	nn	L36852-C-X	RESISTOR 0R0 (Res-Type8)
C65	nn	L50653-C9470-J5	CAPACITOR 47P (Cap-Type10)
C65	R4004	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
C65	R4019	L50652-C391-J2	RESISTOR 390 (Res-Type10)
C65	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C65	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C65	V1304	L36830-C1121-D670	TRANSISTOR FDG313N (Tra-Type5)
C65	V1305	L36830-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)
C65	V1400	L36840-D66-D670	DIODE BAV99T (Di-Type5)
C65	V1500	L36840-C4057-D670	TRANSISTOR EMD12 EMT6 (Tra-Type8)
C65	V1605	L36840-D3088-D670	DIODE SC89 (Di-Type2)
C65	V2100	L36840-D66-D670	DIODE BAV99T (Di-Type5)
C65	V2302	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C65	V2303	L36840-C4059-D670	TRANSISTOR 2*PNP (Tra-Type9)
C65	V2821	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C65	V4001	L50640-C4049-D670	TRANSISTOR SOT-363 (Tra-Type11)
C65	V4002	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
C65	Z1000	L36145-F102-Y21	QUARZ 32,768KHZ (Q-Type2)
C65	Z1500	L36820-L6147-D670	FILTER EMI (Fi-Type4)

C65	Z4001	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)
C65	Z4011	L50645-K260-Y79	BALUN 1710-1910 MHZ
C65	Z4012	L50645-K260-Y80	BALUN 880-915 MHZ

2 List of available level 3 parts C70IFX

Product	ID	Order Number	Description CM
C70	C1000	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1123	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1200	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1201	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1202	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1203	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1204	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1205	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1206	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1207	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1208	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1209	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1211	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1302	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1303	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1304	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1308	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1309	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1310	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1311	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1312	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1313	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1314	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1315	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1317	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1318	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1319	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1329	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1330	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1331	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1332	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
C70	C1355	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)

C70	C1356	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
C70	C1381	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C1382	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C2232	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3600	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3601	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3602	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3603	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3610	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3621	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3804	L50653-C9060-D805	CAPACITOR 3P3 (Cap-Type9)
C70	C3924	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3930	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3931	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3932	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3934	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3966	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3987	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	C3988	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C70	D1000	L36810-G6191-D670	IC SGOLDLITE PMB8875 V1X
C70	D1300	L36145-J4683-Y19	IC ASIC D1094DA MOZART/TWIGO4
C70	D3601	L36820-U6054-D670	IC CAMERA INTERFACE S1D13716B02
C70	D4001	L50610-L6111-D670	IC TRANCEIVER PMB6270 SMARTI SD
C70	D4031	L50645-K280-Y277	IC FEM EPCOS 900 1800 1900MHZ (Fem-Type4)
C70	L1300	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C70	L1301	L36151-F5103-M3	COIL 10U (Co-Type1)
C70	L1302	L36151-F5472-M1	COIL 4U7 (Co-Type3)
C70	L1318	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C70	L1331	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C70	N1501	L36810-B6132-D670	IC LOGIC DUAL BUS SWITCH US8
C70	N3600	L36810-C6134-D670	IC V-REG 2.9V (Vr-Type1)
C70	N3981	L50651-Z2002-A78	IC MODUL PA PF0814 (PA-Type2)
C70	nn	L36852-C-X	RESISTOR 0R0 (Res-Type8)
C70	nn	L50653-C9470-J5	CAPACITOR 47P (Cap-Type10)
C70	R4004	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
C70	R4019	L50652-C391-J2	RESISTOR 390 (Res-Type10)
C70	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C70	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C70	V1304	L36830-C1121-D670	TRANSISTOR FDG313N (Tra-Type5)
C70	V1305	L36830-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)
C70	V1400	L36840-D66-D670	DIODE BAV99T (Di-Type5)

C70	V1500	L36840-C4057-D670	TRANSISTOR EMD12 EMT6 (Tra-Type8)
C70	V1605	L36840-D3088-D670	DIODE SC89 (Di-Type2)
C70	V2100	L36840-D66-D670	DIODE BAV99T (Di-Type5)
C70	V2302	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C70	V2303	L36840-C4059-D670	TRANSISTOR 2*PNP (Tra-Type9)
C70	V2821	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C70	V4001	L50640-C4049-D670	TRANSISTOR SOT-363 (Tra-Type11)
C70	V4002	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
C70	Z1000	L36145-F102-Y21	QUARZ 32,768KHZ (Q-Type2)
C70	Z1500	L36820-L6147-D670	FILTER EMI (Fi-Type4)
C70	Z4001	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)
C70	Z4011	L50645-K260-Y79	BALUN 1710-1910 MHZ
C70	Z4012	L50645-K260-Y80	BALUN 880-915 MHZ

3 List of available level 3 parts CX70IFX

Product	ID	Order Number	Description CM
CX70	C1304	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1315	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1318	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1329	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1330	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1332	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	C1355	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
CX70	C1356	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
CX70	C3906	L36344-F1225-M12	CAPACITOR 2*2U2 (Cap-Type7)
CX70	D1000	L36810-G6191-D670	IC SGOLDLITE PMB8875 V1X
CX70	D1300	L36145-J4683-Y19	IC ASIC D1094DA MOZART/TWIGO4
CX70	D3601	L36820-U6052-D670	IC CAMERA INTERFACE S1D13716B01
CX70	D4001	L50610-L6111-D670	IC TRANCEIVER PMB6270 SMARTI SD
CX70	D4031	L50645-K280-Y277	IC FEM EPCOS 900 1800 1900MHZ (Fem-Type4)
CX70	L1300	L36140-F2100-Y6	COIL 0603 (Co-Type4)
CX70	L1301	L36151-F5103-M3	COIL 10U (Co-Type1)
CX70	L1302	L36151-F5472-M1	COIL 4U7 (Co-Type3)
CX70	L1318	L36140-F2100-Y6	COIL 0603 (Co-Type4)
CX70	L1331	L36140-F2100-Y6	COIL 0603 (Co-Type4)
CX70	N1501	L36810-B6132-D670	IC LOGIC DUAL BUS SWITCH US8
CX70	N3600	L36810-C6065-D670	IC VRGLU 2,8V
CX70	N3981	L50651-Z2002-A78	IC MODUL PA PF0814 (PA-Type2)
CX70	nn	L36852-C-X	RESISTOR 0R0 (Res-Type8)

CX70	nn	L50653-C9470-J5	CAPACITOR 47P (Cap-Type10)
CX70	R4004	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
CX70	R4019	L50652-C391-J2	RESISTOR 390 (Res-Type10)
CX70	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
CX70	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
CX70	V1304	L36830-C1121-D670	TRANSISTOR FDG313N (Tra-Type5)
CX70	V1305	L36830-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)
CX70	V1400	L36840-D66-D670	DIODE BAV99T (Di-Type5)
CX70	V1500	L36840-C4057-D670	TRANSISTOR EMD12 EMT6 (Tra-Type8)
CX70	V1605	L36840-D3088-D670	DIODE SC89 (Di-Type2)
CX70	V2302	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
CX70	V2303	L36840-C4059-D670	TRANSISTOR 2*PNP (Tra-Type9)
CX70	V2404	L36830-C1112-D670	TRANSISTOR SI1902 (Tra-Type4)
CX70	V2821	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
CX70	V3961	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
CX70	V4001	L50640-C4049-D670	TRANSISTOR SOT-363 (Tra-Type11)
CX70	Z1000	L36145-F102-Y21	QUARZ 32,768KHZ (Q-Type2)
CX70	Z1500	L36820-L6147-D670	FILTER EMI (Fi-Type4)
CX70	Z4001	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)
CX70	Z4011	L50645-K260-Y79	BALUN 1710-1910 MHZ
CX70	Z4012	L50645-K260-Y80	BALUN 880-915 MHZ

4 List of available level 3 parts C72IFX

Product	ID	Order Number	Description CM
C72	C1000	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1123	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1200	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1201	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1202	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1203	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1204	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1205	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1207	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1208	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1209	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1211	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1302	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1303	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1308	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)

C72	C1309	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1310	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1311	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1312	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1313	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1314	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1317	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1319	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1355	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
C72	C1356	L50675-F3475-K	CAPACITOR 4U7 (Cap-Type12)
C72	C1381	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C1382	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C2232	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3600	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3601	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3602	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3603	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3610	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3621	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C3988	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C4001	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	C4012	L50653-C9040-C705	CAPACITOR 4P7 (Cap-Type14)
C72	C4040	L36853-C9104-M4	CAPACITOR 100N (Cap-Type2)
C72	D1000	L50610-G6196-D670	IC SGOLDLITE PMB8875 V1X PB-FREE
C72	D1300	L50697-F5013-F202	IC ASIC MOZART PB-FREE
C72	D3601	L36820-U6054-D670	IC CAMERA INTERFACE S1D13716B02
C72	D4001	L50610-L6111-D670	IC TRANCEIVER PMB6270 SMARTI SD
C72	D4031	L50645-K280-Y277	IC FEM EPCOS 900 1800 1900MHZ (Fem-Type4)
C72	L1300	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C72	L1301	L36151-F5103-M3	COIL 10U (Co-Type1)
C72	L1302	L36151-F5472-M1	COIL 4U7 (Co-Type3)
C72	L1318	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C72	L1331	L36140-F2100-Y6	COIL 0603 (Co-Type4)
C72	N1501	L36810-B6132-D670	IC LOGIC DUAL BUS SWITCH US8
C72	N3600	L50610-C6187-D670	IC V-REG 2.5V PB FREE
C72	N3981	L50651-Z2002-A82	IC MODUL PA PF0814 (PA-Type3) PB Free
C72	R4004	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
C72	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C72	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
C72	V1304	L36830-C1121-D670	TRANSISTOR FDG313N (Tra-Type5)
C72	V1305	L36830-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)

C72	V1400	L36840-D66-D670	DIODE BAV99T (Di-Type5)
C72	V1500	L36840-C4057-D670	TRANSISTOR EMD12 EMT6 (Tra-Type8)
C72	V1605	L36840-D3088-D670	DIODE SC89 (Di-Type2)
C72	V2100	L36840-D66-D670	DIODE BAV99T (Di-Type5)
C72	V2302	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C72	V2303	L36840-C4059-D670	TRANSISTOR 2*PNP (Tra-Type9)
C72	V2821	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
C72	V4001	L50640-C4049-D670	TRANSISTOR SOT-363 (Tra-Type11)
C72	V4002	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
C72	Z1000	L50645-F102-Y40	QUARZ 32,768KHZ (Q-Type4)
C72	Z1500	L50620-L6151-D670	FILTER EMI (Fi-Type5) PB Free
C72	Z4001	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)
C72	Z4011	L50645-K260-Y79	BALUN 1710-1910 MHZ
C72	Z4012	L50645-K260-Y80	BALUN 880-915 MHZ

5 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A1)
- Troubleshooting Frame C65 (F30032-P377-A1)
- Troubleshooting Frame CX65, M65 (F30032-P343-A1)
- Power Supply (at least one GRT required power supply)
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

Reference: Equipment recommendation Version X (newest version)
(downloadable from the technical support page)

6 Required Software for Level 3 C65, C70, CX70, C72

- XFocus for 65series
- Software for GSM-Tester (GRT)
- Software for reference oscillator adjustment
- Internet unblocking solution (JPICS)
- Dongle driver for dongle protected Siemens software tools

7 Radio Part

The radio part realizes the conversion of the GMSK-HF-signals from the antenna to the base-band and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

Transmitter and Receiver are never active at the same time. Simultaneous receiving in two bands is impossible. Simultaneous transmission in two bands is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

The RF-part of the is dimensioned for triple band operation (EGSM900, GSM1800, GSM1900) supporting GPRS functionality up to multiclass 10.

The RF-circuit consists of the following components:

Infineon Smarti SD chip set PMB6270

- PLL for local oscillator LO1 (no further VCOs required due to digital modulation)
- Integrated local oscillator LO1-VCO (without loop filter)
- Direct conversion receiver including LNA, DC-mixer, channel filtering and baseband amplifier

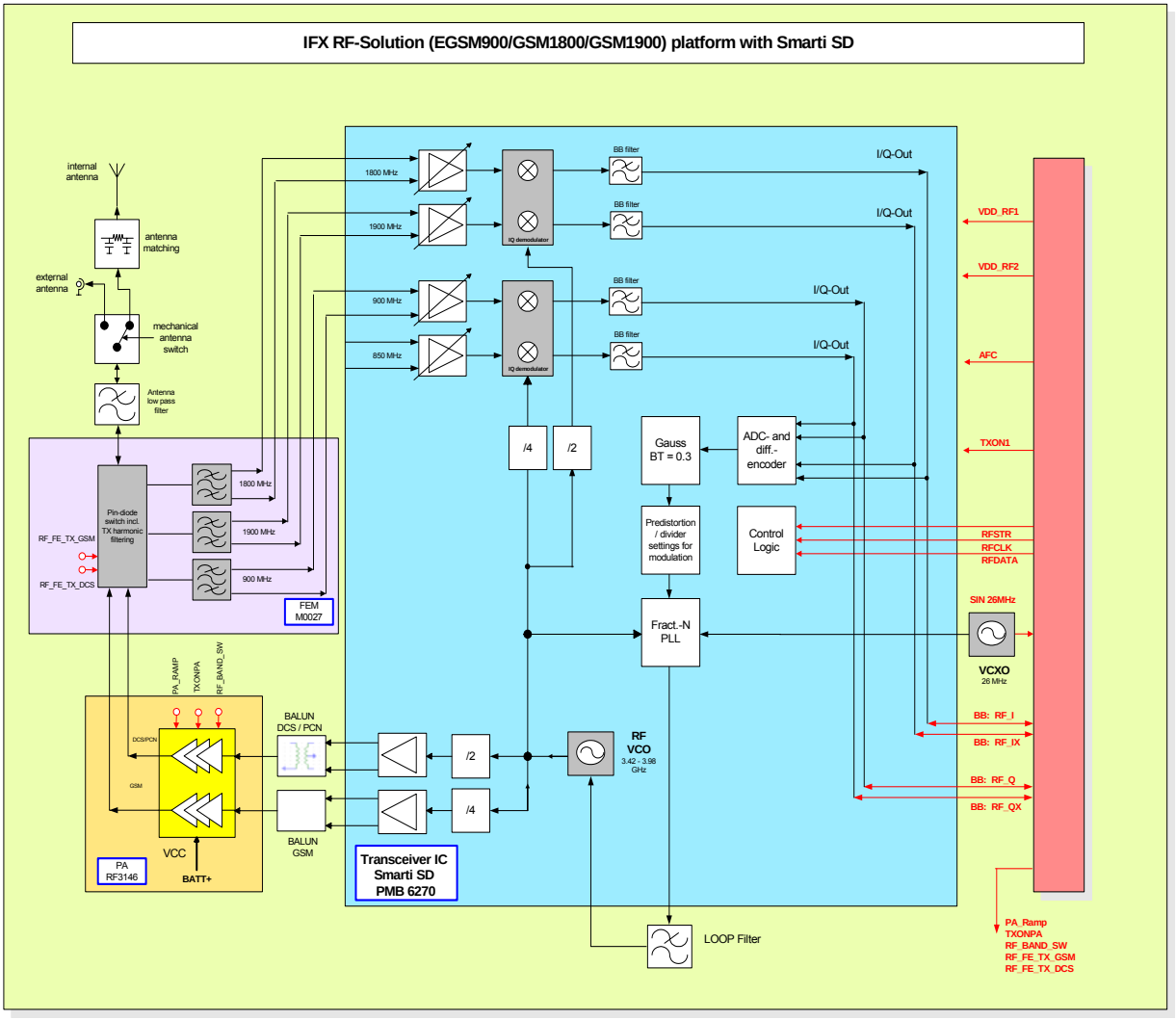
Digital Modulator by fast Sigma Delta PLL and integrated AD-converters for TX Baseband signals

RF Micro Devices transmitter PA RF3146 (incl. integrated power control circuitry)

Epcos Front -End-Module (FEM) M0027 including RX-/TX-switch and EGSM 900/GSM1800/ GSM1900 receiver SAW-filters

Quartz and passive circuitry of the 26MHz VCXO reference oscillator.

7.1 Block diagram RF part

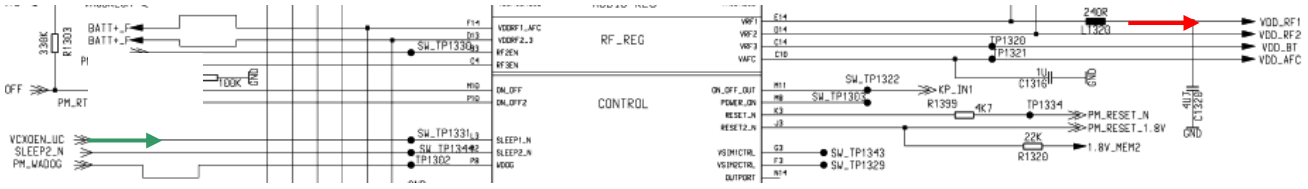


7.2 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D1300.(see chapter 5.2).It generates the required 2,85V “RF-Voltage” named VDD_RF1(VDD_BRIGHT). The voltage regulator is activated as well as deactivated via VCXOEN_UC (Functional F23) provided by the SGOLDLITE+. The temporary deactivation is used to extend the stand by time.

Circuit diagram

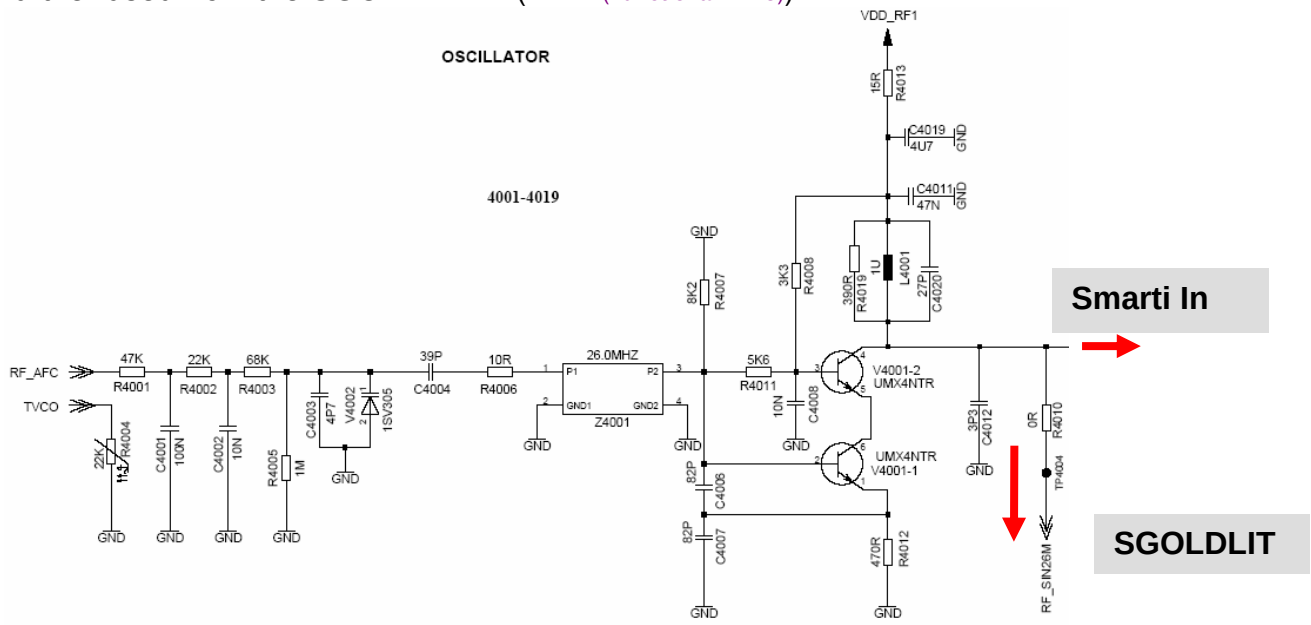
VDD_RF1



7.3 Frequency generation

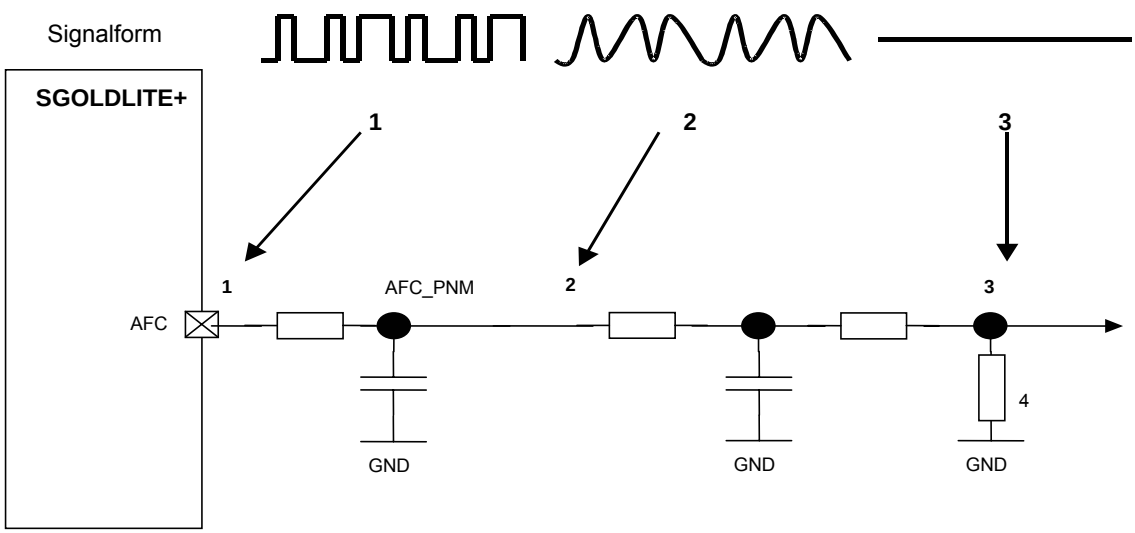
7.3.1 Synthesizer: The discrete VCXO (26MHz)

The mobiles are using a reference frequency of 26MHz. The generation of the 26MHz signal is done via a VCXO. This oscillator consists mainly of:
The oscillator output signal 26MHz_RF is connected via a puffer station to the transceiver to be used as reference frequency. The signal leaves is also connected as RF_SIN26M to be further used from the SGOLDLITE+ (D171 (Functional AE15)).



To compensate frequency drifts (e.g. caused by temperature) the oscillator frequency is controlled by a (RF_AFC) signal, generated through the internal SGOLDLITE+. PLL via the capacity diode. Reference for the “SGOLDLITE-PLL” is the base station frequency received via the Frequency Correction Burst. To compensate a temperature caused frequency drift, the temperature-depending resistor is placed near the VCXO to measure the temperature. The measurement result TVCXO is reported to the SGOLDLITE+.

Waveform of the AFC_PNM signal from SGOLDLITE+ to Oscillator



7.3.2 Local Oscillator (LO1)

The local oscillator (LO1) consists of a 23-bit fractional-N PLL and the VCO, both integrated in the Smarti SD and an external loop filter. The PD frequency is 26MHz. An LO2 is not required. The frequency range of the VCO is 3420MHz to 3980MHz for the triple-band phone. Therefore the LO frequency is 4 times the RX/TX frequency for GSM 900 and 2 times RX/TX frequency for GSM 1800/1900.

The VCO has 2048 bands that are chosen by the ‘binary automatic band select’ BABS at the PLL start with the Reg1 programming word. After the BABS the ‘open loop gain adjust’ OLGA sets two charge pump currents and measures the corresponding VCO frequency. So the system knows the result of a loop gain relevant parameter and adjusts it automatically by the programmable charge pump current. After this adjustment the analog locking starts. The total lock time of 90µs (typical) consists of about 65µs for BABS and OLGA and about 20µs for the following analog locking. The worst case specified lock time is 200µs. So the synthesizer is capable of GPRS class 12. Due to the automatic band select with the fine VCO bands the tune voltage stays normally quite constant over the channels between 200mV and 250mV.

The GMSK modulation for TX is injected by adapting the divider value of the PLL very fast with the desired modulation.

7.3.3 Receiver

The Smarti SD consists of a direct conversion receiver for GSM850/900/1800/1900. However, the GSM850 chain will not be used in this project.
The GSM900/1800/1900 LNAs with balanced inputs are integrated into the chip. The LNA gain is switchable. For the “High Gain” state the mixers are optimised for conversion gain and noise figure, in the “Low Gain” state the mixers are optimised to large signal behaviour for operation at a high input level. The gain step for the LNA is approximately 34dB for all three bands. There is another fixed gain precision amplifier with 6dB that will be switched on at reference sensitivity level (-90dBm input level) to avoid accuracy losses at very low input levels.
A quadrature demodulator converts the amplified RF signal to the final orthogonal output signals at baseband frequency. The orthogonal LO signals are generated by a divider by 4 for the GSM900 band and by a divider by 2 for the GSM1800 and GSM1900 band.
The resulting in-phase and quadrature signals are fed into the baseband low pass filters providing sufficient suppression of blocking signals as well as of adjacent channel interferers and ensures the ADC's anti-aliasing requirements at 13MHz clock rate. A programmable gain stage for the correction of gain tolerances in fourteen 1dB steps (-6dB…+7dB) and the adaptation of the output signals to the baseband ADC's input dynamic range is implemented.
The IQ receiver signals are fed into the AD converters of the SGOLDlite and the differential baseband signals are digitalised separately for the I and Q path. On SGOLDlite both the digital and analogue baseband filters of the I/Q-interface are implemented. The analogue part of the baseband receive section comprises anti-aliasing pre-filters for in-phase and quadrature components and $\Sigma\Delta$ analogue-to-digital converters with approximately 12 bit (standard mode) and 14 bit (enhanced mode) resolution with 2 Vpp max differential input voltage. The complete ADC functionality comprises the ADC and the digital baseband receive filters.
The baseband receive filters are digital multi rate decimation low pass filters. They consist of several filter stages with decimations taking place as early as possible. The last filter stage is an adaptive switchable linear-phase FIR filter. Depending on the level of adjacent channel interference it selects a filter with appropriate frequency transfer characteristic for improved channel filtering. Furthermore, the filter coefficients of the last FIR filter stage are programmable for optimisation purposes.

7.3.4 Transmitter (Sigma Delta)

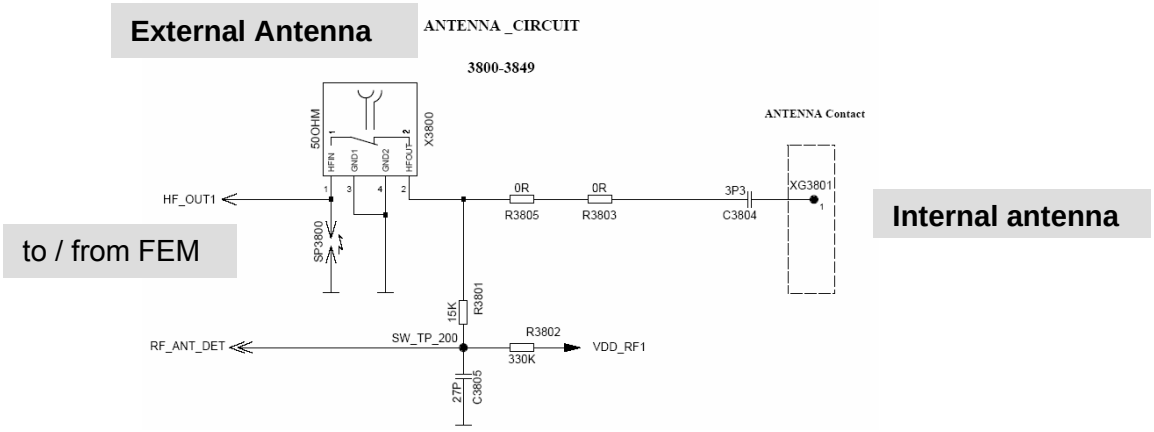
The Smarti SD uses a new digital modulation principle. Basis is the fact, that the GMSK modulation can be considered to be a phase modulation in its origin. It can be achieved by controlling the frequency of a VCO. There are various methods to do so. One of the smartest is to use a PLL for this application. The advantage of this method is a low effort in hardware and that a lot of unwanted spurs are not generated e.g. carrier- or sideband spurs. So a calibration of the sideband- and carrier during production is not necessary any longer.
The I-/Q- signals are provided by the base band chipset with a 1.0V DC offset and amplitude of 0.94Vpp over balanced lines. The first step now is to convert the base band signal from analog to digital. After that the signal passes a digital gaussian filter and is fed to the mash modulator. This network is calculating the divider settings of the PLL. The VCO is oscillating from 3.42 GHz to 3.98 GHz. This is twice the frequency for the high band, so a division by 2 is necessary for DCS/PCS operation and a division by 4 for GSM 900 operation.The output signal of the modulator is buffered with two different stages for GSM and DCS/PCS. The output is balanced. The transformation to an unbalanced signal is done with a subsequent balun. The final adaptation of the input power for the PA is made with an attenuator that follows after the balun. After that, the signal is fed to the PA.

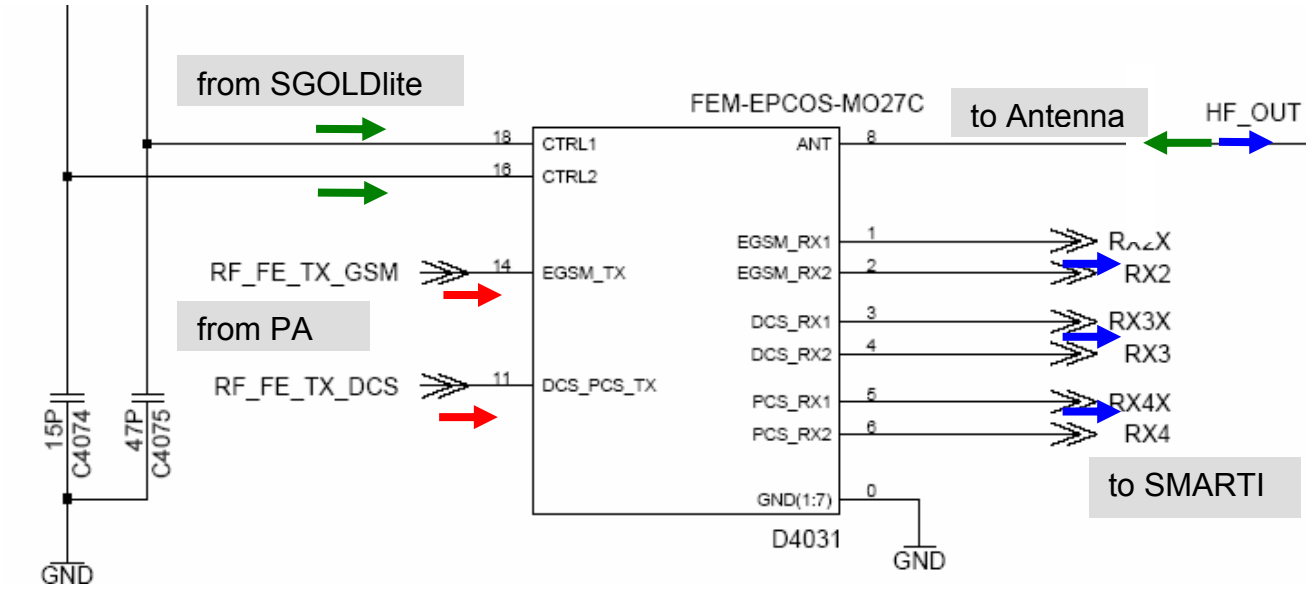
7.4 Antenna switch (electrical/mechanical)

Internal/External <> Receiver/Transmitter
The mobile have two antenna switches.

a) The mechanical antenna switch for the differentiation between the internal and external antenna, which is used only RF adjustment.
b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals.

To activate the correct settings of this diplexer, the SGOLDLITE+ signals
RF_FE_DTR_GSM and RF_FE_DTR_DCS are required



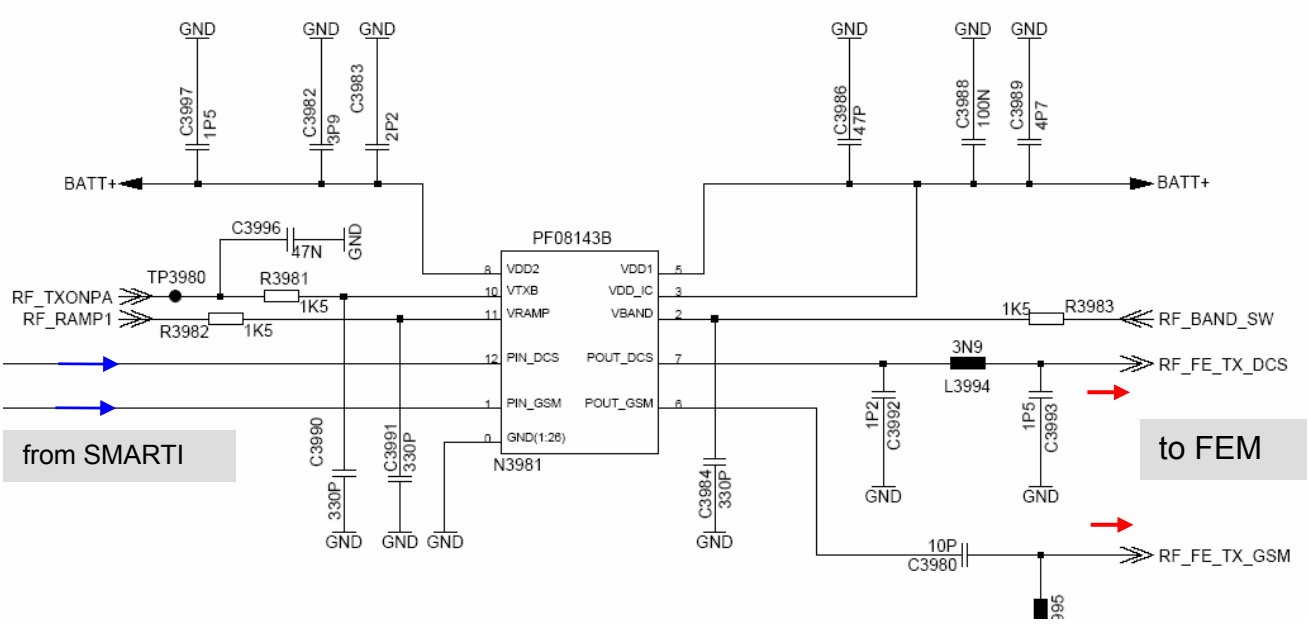

from SGOLDlite
FEM-EPCOS-MO27C
to Antenna
HF_OUT
18
CTRL1
ANT
8
16
CTRL2
EGSM_RX1
1
RX1X
RF_FE_TX_GSM
14
EGSM_TX
EGSM_RX2
2
RX2
from PA
DCS_RX1
3
RX3X
DCS_RX2
4
RX3
RF_FE_TX_DCS
11
DCS_PCS_TX
PCS_RX1
5
RX4X
PCS_RX2
6
RX4
to SMARTI
GND(1:7)
0
15P
C4074
47P
C4075
D4031
GND
GND

7.4.1 Transmitter: Power Amplifier

The output signals from the tranceiver are led to the power amplifier via balluns. The power amplifier is a module from RF Micro Devices and matched to 50 Ω at all signal ports. It contains two separate 3-stage amplifier chains for EGSM900 and GSM1800/GSM1900. It is possible to control the output-power of both bands via one VAPC-port. The appropriate amplifier chain is activated by a logic signal provided from the baseband. To ensure that the output power and burst timing fulfills the GSM-specification the power-controller is as well integrated in the module. The combination of antenna, antenna LPF, FEM and transmission lines will prevent the PA of critical mismatch phases. The power-controller itself is controlled by the PA-Ramp signal provided by the baseband.

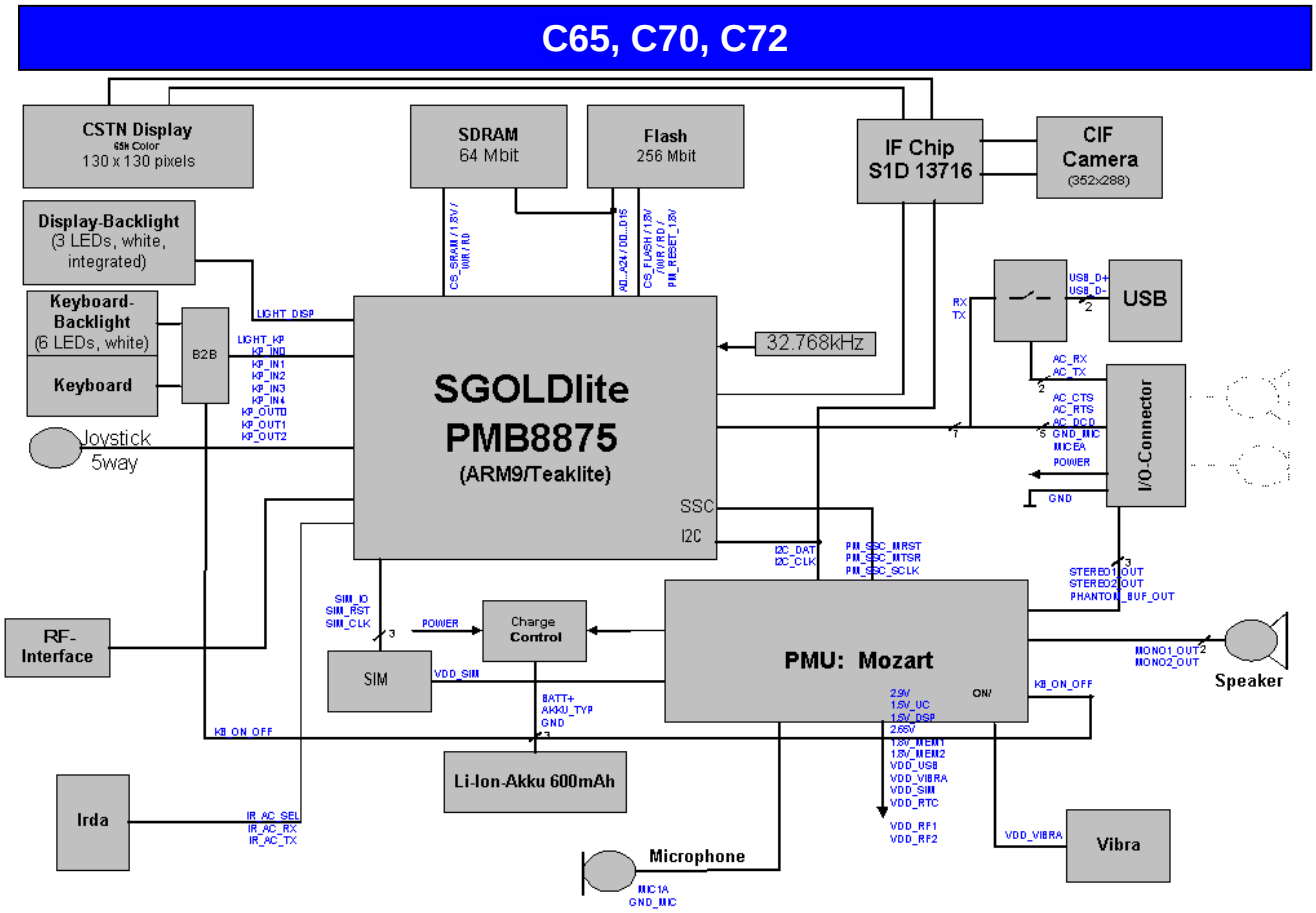
The required voltage BATT+ is provided by the battery.

Circuit diagram

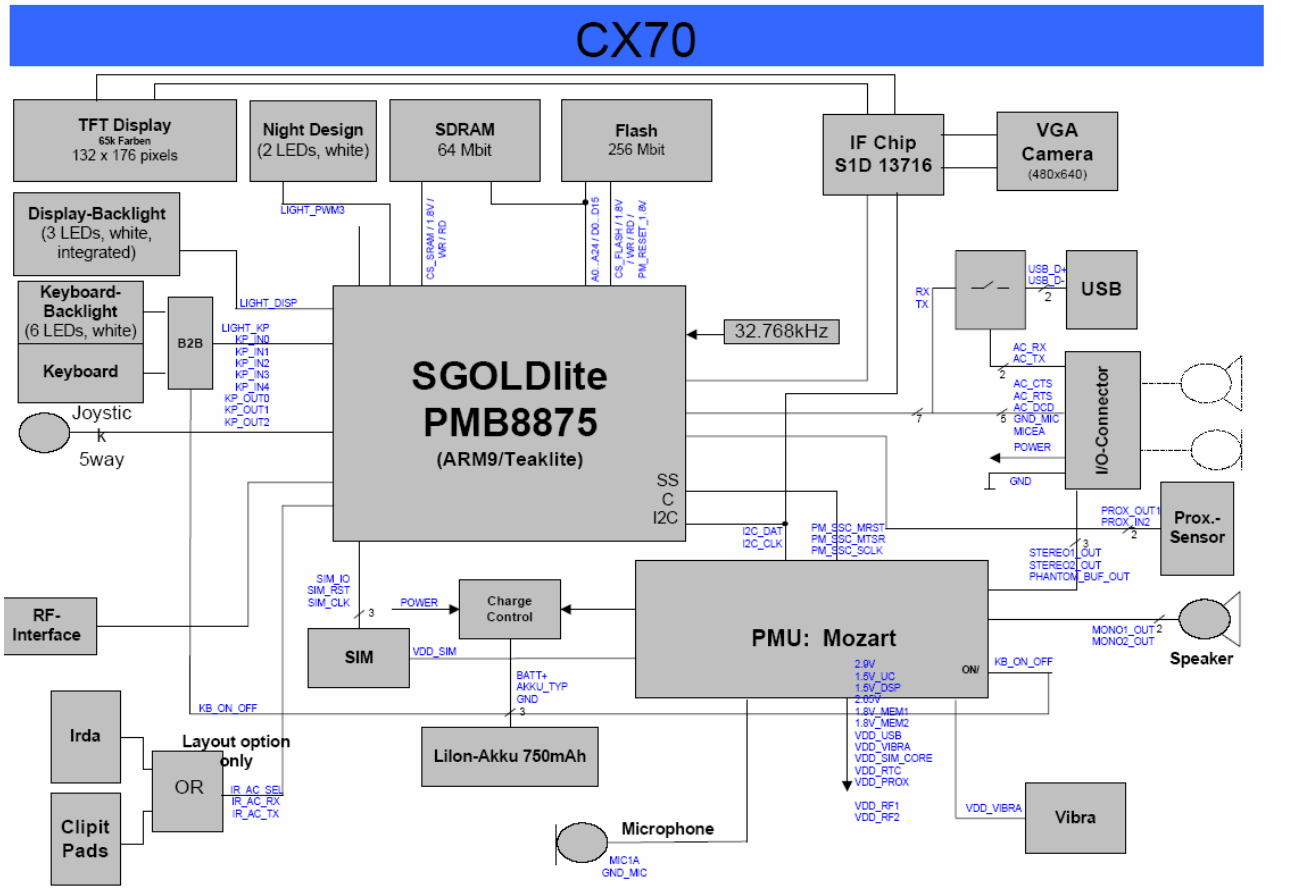


8 Logic / Control

8.1 Logic Block Diagram C65, C70, C72



8.2 Logic Block Diagram CX70



8.3 SGOLDLITE

8.3.1 Digital Baseband

Baseband Processor SGOLDlite (PMB8875)

S-GOLDliteTM is a GSM single chip mixed signal baseband IC containing all analog and digital functionality of a cellular radio. The integrated circuit contains a ARM926EJ-S CPU and a TEAKLite DSP core. The ARM926EJ-S is a powerful standard controller and particularly suited for wireless systems. It is supported by a wide range of tools and application SW. The TEAKLite is an established DSP core for wireless applications with approved firmware for GSM signal processing. The package is a P-LFBGA-345 (264 functional pins + 81 thermical balls).

Supported Standards

- GSM speech FR, HR, EFR and AMR-NB
- GSM data 2.4kbit/s, 4.8kbit/s, 9.6kbits, and 14.4kbit/s
- HSCSD class 10
- GPRS class 12

Processing cores

- ARM926EJ-S 32-bit processor core with operating frequency up to 125 MHz for controller functions
- TEAKLite DSP core with operating frequency 104 MHz.

ARM-Memory

- 8 kByte Boot ROM on the AHB
- 96 kByte SRAM on the AHB, flexibly usable as program or data RAM
- 8 kByte Cache for Program (internal)
- 8 kByte tightly coupled memory for Program (internal)
- 8 kByte Cache for Data (internal)
- 8 kByte tightly coupled memory for Data (internal)

TEAKLite-Memory

- 80 kwords Program ROM
- 4 kwords Program RAM
- 48 kwords Data ROM
- 27 kwords Data RAM

Shared Memory Blocks

- 1.5 kwords Shared RAM (dual ported) between controller system and TEAKLite.

Functional Hardware blocks

- CPU and DSP Timers
- Programmable PLL with additional phase shifters for system clock generation
- GSM Timer Module that off-loads the CPU from radio channel timing
- GMSK Modulator according to GSM-standard 05.04 (5/2000)
- Hardware accelerators for equalizer and channel decoding
- Advanced static and dynamic power management features including TDMA-Frame synchronous low-power mode and enhanced CPU modes (idle and sleep modes)

Interfaces and Features

- Keypad Interface for scanning keypads up to 6 rows and 4 columns
- Pulse Number Modulation output for Automatic Frequency Correction (AFC)
- Serial RF Control Interface; support of direct conversion RF
- 2 USARTs with autobaud detection and hardware flow control
- IrDA Controller integrated in USART0 (with IrDA support up to 115.2 kbps)
- 1 Serial Synchronous SPI compatible interfaces in the controller domain
- 1 Serial Synchronous SPI compatible interface in the TEAKLite domain
- I2C-bus interface (e.g. connection to S/M-Power)
- 2 bidirectional and one unidirectional I2S interface accessible from the TEAKLite
- USB V1.1 mini host interface for full speed devices with up to 5 interfaces and 10 endpoints configurable supporting also USB on-the-go functionality
- ISO 7816 compatible SIM card interface
- Enhanced digital (phase linearity, adj/ co-channel interference) baseband filters, including analog prefilters and high resolution analog-to-digital converters.
- Separate analog-to-digital converter for various general purpose measurements like battery voltage, battery, VCXO and environmental temperature, battery technology, transmission power, offset, onchip temperature, etc.
- Ringer support for highly oversampled PDM/PWM input signals for more versatility in ringer tone generation
- RF power ramping functions
- DAI Interface according to GSM 11.10 is implemented via dedicated I2S mode
- 26 MHz master clock input
- External memory interface:
  - 1.8V interface
  - Data bus: 16 bit non-multiplexed and multiplexed, 32 bit multiplexed
  - Supports synchronous devices (SDRAMs and Flash Memory) up to 62.4 MHz
  - For each of the 4 address regions 128 MByte with 32-bit access or 64 MByte with a 16-bit access are addressable

  - Supports asynchronous devices (i.e. SRAM, display) including write buffer for cache line write
- Port logic for external port signals
- Comprehensive static and dynamic Power Management
  - Various frequency options during operation mode
  - 32 kHz clock in standby mode
  - Sleep control in standby mode
  - RAMs and ROMs in power save mode during standby mode
  - Additional leakage current reduction in standby mode possible by switching off the power for the TEAKLite subsystem.

Baseband receive path

In the receiver path the antenna input signal is converted to the base band, filtered, and amplified to target level by the RF transceiver chipset. The resulting differential I and Q baseband signals are fed into the S-GOLDliteTM. The A-to-D converter generates two 6.5 Mbit/s data streams. The decimation and narrowband channel filtering is done by a digital baseband filter for each path. The DSP performs for GMSK, the complex baseband signal equalization with soft-output recovery and the channel decoding supported by a Viterbi hardware accelerator. The recovered digital speech data is fed into the speech decoder (D1300). The S-GOLDliteTM supports fullrate, halfrate, enhanced fullrate and adaptive multirate speech codec algorithms.

Baseband transmit path

In the transmit direction the microphone signal is amplified and A-to-D converted by the D1300. The prefiltered and A-to-D converted voice signal passes a digital decimation filter. Speech and channel encoding (including voice activity detection, VAD, and discontinuous transmission, DTX) as well as digital GMSK modulation is carried out by the S-GOLDliteTM. The digital I and Q baseband components of the GMSK modulated signals (48-times oversampled with 13 MSamples/s) are D-to-A converted. The analog differential baseband signals are fed into the RF transceiver chipset. The RF transceiver modulates the baseband signal using a GMSK modulator. Finally, an RF power module amplifies the RF transmit signal to the required power level. The S-GOLDliteTM controller software controls the gain of the power amplifier by predefined ramping curves (16 words, 11 bit). The S-GOLDliteTM communicates with the RF chip set via a serial data interface.

The following algorithms and a task scheduler are implemented on the DSP:
Algorithms running on the DSP:

- scanning of channels, i.e, measurement of the field strengths of neighbouring base stations
- detection and evaluation of Frequency Correction Bursts
- equalisation of GMSK Normal Bursts and Synchronisation Bursts with bit-by-bit soft-output
- Synch burst channel decoder
- channel encoding and soft-decision decoding for fullrate, enhanced-fullrate and adaptive multirate speech, and control channels as well as RACH, PRACH
- channel encoding for GPRS coding schemes (CS1-CS4) as well as USF detection algorithms for the Medium Access Control (MAC) software layer
- fullrate, enhanced fullrate and adaptive multirate speech encoding and decoding
- support for fullrate (F9.6, F4.8, and F2.4) data channels
- mandatory sub-functions like
  – discontinuous transmission,
  – voice activity detection, VAD
  – background noise calculation
- generation of tone and side tone
- hands-free functions (acoustic echo cancellation, noise-reduction)
- support for voice memo
- support for voice dialling
- handling of vocoder and voice-paths for type approval testing
- ADPCM encoder (8 kHz sampling frequency), cannot run in parallel to a speech codec
- ADPCM decoder (8 kHz and 16 kHz sampling frequency), cannot run in parallel to a speech codec

Scheduler functions on the DSP:
The scheduler is based on an operating system. It is basically triggered by interrupts generated by hardware peripherals or commands from the micro-controller.

- communication between DSP and micro-controller
- fully automatic handling of speech channels
- semi-automatic handling of control channels
- support of the GSM ciphering algorithm (A51, A52, A53) in combination with the hardware accelerator.
- support for General Packet Radio Services (GPRS) with up to 4 Rx and 1Tx or 3 Rx and 2 Tx (Class 10 mobile).
- monitoring of paging blocks for packet switched and circuit switched services simultaneously GPRS MS in Class-B mode of operation
- MMS support
- loop-back functions (according to GSM 11.10)

Real Time Clock
The real time clock (degree of accuracy 150ppm) is powered via a separate voltage regulator inside the ASIC. Via a capacitor, data is kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with which it is possible to switch the phone on and off.

Measurement of Battery voltage, Battery Type and Ambient Temperature
The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor and the ambient temperature.

Timing of the Battery Voltage Measurement
Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

8.3.2 SDRAM

Memory for volatile data. SDRAM= synchronous High data rate Dynamic RAM

Memory Size:	64 Mbit
Data Bus:	16 Bit
Frequency:	105 MHz
Power supply:	1.8 V

8.3.3 FLASH

Non-volatile but deletable and re-programmable (software update) program memory for the S-GOLDlite and for saving e.g. user data (menu settings), voice band data (voice memo), mobile phone matching data, images etc.. There is a serial number on the flash which cannot be changed.

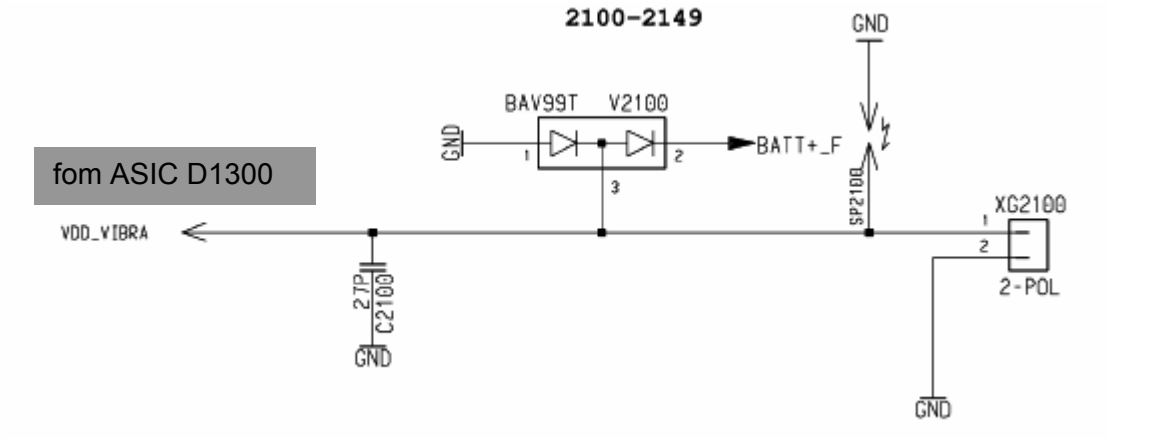
Memory Size	256 Mbit (32 MByte)
Data Bus:	16 Bit
Access Time:	Initial access: 85 ns
Synchronous Burst Mode:	54 MHz / 14ns clock to data output
Asynchronous Mode:	85 ns

8.3.4 SIM

SIM cards with supply voltages of 1.8V and 3V are supported. 1.8V cards are supplied with 3V.

8.3.5 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts.



9 Power Supply

9.1 ASIC Mozart / Twigo4

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- 17 Voltage regulators
- 2 internal DC/DC converters (Step-up and Step-down converter)
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I^2C interface)
- Bandgap reference
- High performance audio quality
- Audio multiplexer for selection of audio input
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I^2S Interface

9.1.1 Battery

As a standard battery a LiIon battery with a nominal capacity of 780mAh@0.2CA* and GSM capacity** of min. 750mAh will be provided.

* battery will be discharged with 20% of capacity rate till 2.75V; e.g. R65, 0.2x750mA=150mA
** battery will be discharged with 2A(0.6ms)+0.25A(0.4ms) till 3.2V.

9.1.2 Charging Concept

9.1.2.1 General

The battery is charged in the phone. The hardware and software is designed for LiIon with 4.2V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the “Charge” symbol in the display). During normal use the phone is being charged (restrictions: see below). Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the ASIC hardware can override/interrupt the charging in the case of over voltage of the battery
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. Charging is ongoing as long the temperature is within the range +5°C to 45°C. The maximal charge time will be 2 hours (I_{max}=750mA).

9.1.2.2 Measurement of Battery voltage, Battery Type and Ambient Temperature

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor and the ambient temperature.

9.1.2.3 Timing of the Battery Voltage Measurement

Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

9.1.2.4 Recognition of the Battery Type

The different batteries will be encoded by different resistors within the battery pack itself.

9.1.2.5 Charging Characteristic of Lithium-Ion Cells

LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is given by the connected charger. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be performed is in the ranges from 0...50°C. Outside this range no charging takes place, the battery only supplies current.

9.1.2.6 Trickle Charging

The ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the ASIC by means of the external FET. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.2V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the ASIC will switch on the phone automatically and normal charging will be initiated by software.

9.1.2.7 Normal Charging (Fast charge)

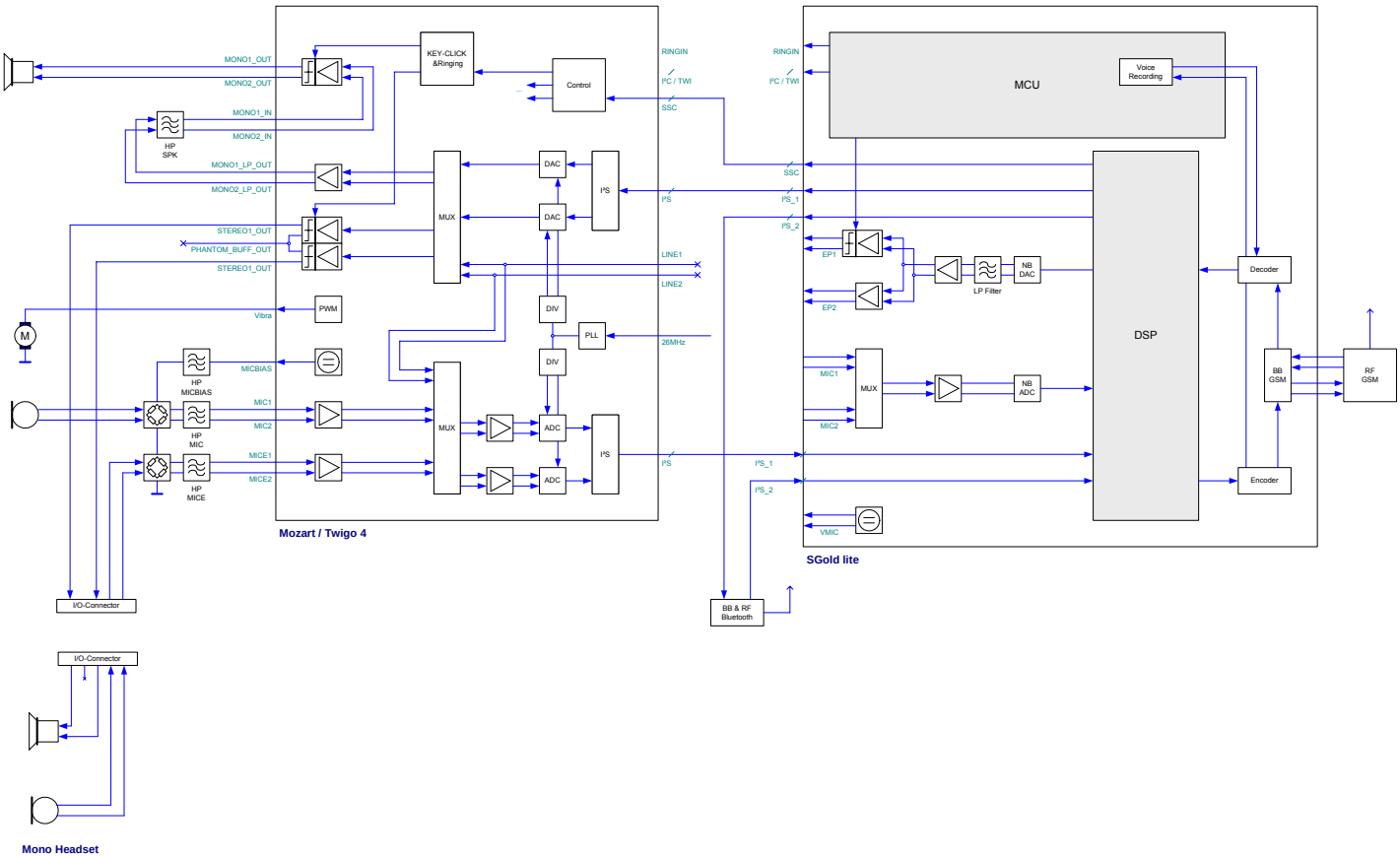
For battery voltages above 3.2 Volt and normal ambient temperature between 0 and 50°C the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the ASIC ASIC. The level of charge current is only limited by the charger.

9.1.2.8 USB Charging

The ASIC can support USB charging when USB charging is integrated in the charging software. If charge voltage is in the range 4.4V to 5.25 V USB charging is ongoing. During USB charging only limited charging is possible. Charge current is limited to 75, 150, 300 or 400 mA.

9.1.2.9 Audio multiplexer

The digital audio information from/to the DSP inside the SGOLD are delivered via the I2S interface, the 26MHz from the RF part. The internal AD and DA converter are connected to microphone and loudspeaker.



9.1.2.10 Interface

The ASIC has two serial control interfaces and one serial audio interface. With the serial interfaces, all functions of the ASIC can be controlled. For time critical commands (all audio functions incl. Vibra) the SSC is used.

TWI interface
TWI (two wire interface) is an I2C 2 wire interface with the signals Clock (I2C_CLK) data line (I2C_DAT) and the interrupt (PM_INT).

SSC interface
The SSC interface enables high-speed synchronous data transfer between SGOLD and ASIC.
The interface consist of: clock signal (PM_SSC_SCLK), master transmit slave receive (PM_SSC_MTSR), master receive slave transmit (PM_SSC_MTSR) and the select line (PM_SSC_CS)

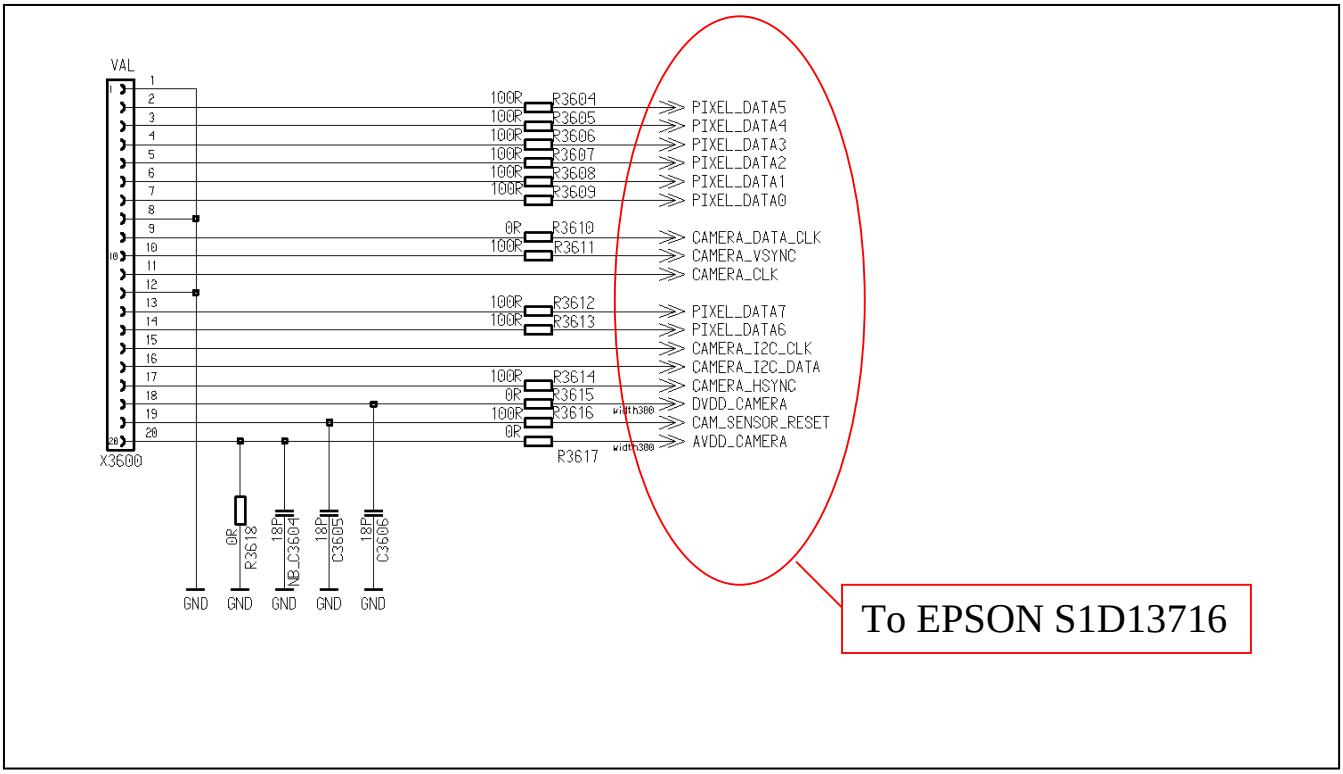
IS2 interface
The audio interface is a bidirectional serial interface, TX and RX part are independent. The IS2 interface consist of a three wire connection for each direction. The three lines are clock (CLK), the serial data line (DAC or ADC) and the word select line (WAO). Clock and word select line is used for RX and TX together in SL65. (PM_I2S_DAC for RX and PM_I2S_ADC for TX)

9.1.2.11 LDO`S

LDO´s:	*Voltage*	*Current*	*Name*	*voltage domains*
REG 1	**2,9V**	0...140mA	2.9V	Display, Epson Camera-Chip, SGOLD
REG 2a	**1,5V**	0...300mA	1.5V_UC	SGOLD
REG 2b	**1,5V**	0...100mA	1.5V_DSP	SGOLD
REG 3	**2,65V**	0...140mA	2.65V	SGOLD, Hall-Sensor, Epson Camera-Chip, USB Switch
MEM REG1	**1,8V**	0...250mA	1.8V_MEM1	SGOLD, Display, SDRAM
MEM REG2	**1,8V**	0...150mA	1.8V_MEM2	Flash Memory, Camera-ASIC
AUDIO REG	**2,9V**	0...190mA	VAUDREGA	PMU ASIC
RF REG1	**2,7V**	0...150mA	VDD_RF1	RF-Part (Hitachi Bright V)
AFC REG	**2,65V**	0...2mA	VDD_AFC	SGOLD
LP_REG	**2,0V**	0...2mA	VDD_RTC	SGOLD
SIM REG	**2,9V**	0...70mA	VDD_SIM	SIM
USB REG	**3,1V**	0...40mA	VDD_USB	SGOLD, USB Protection
VIBRA	**2,8V**	0...140mA	VDD_VIBRA	VIBRA

10 Camera

The camera module uses a color sensor with a full VGA (640x480) resolution in landscape orientation. The module will deliver an 8Bit output signal which will be pre-processed by the EPSON S1D13716 graphic engine chip. Various settings like brightness, image stabilization, white balance can be done by using the I2C interface.



Camera Board-to-Board Connector

11 Camera – Display Interface Module

For the interface between S-GOLDlite, camera and display a graphics engine chip called S1D13716 from Epson is used. By using the SSC interface the S-GOLDlite communicates with this graphic engine chip. The S1D13716 has a second SSC interface to adapt the display. Over an I2C interface, provided by the S1D13716, the camera-module can be initialised; the picture-data output of the camera goes over a parallel 8-bit interface
There are three modes available:

a) Bypass mode:

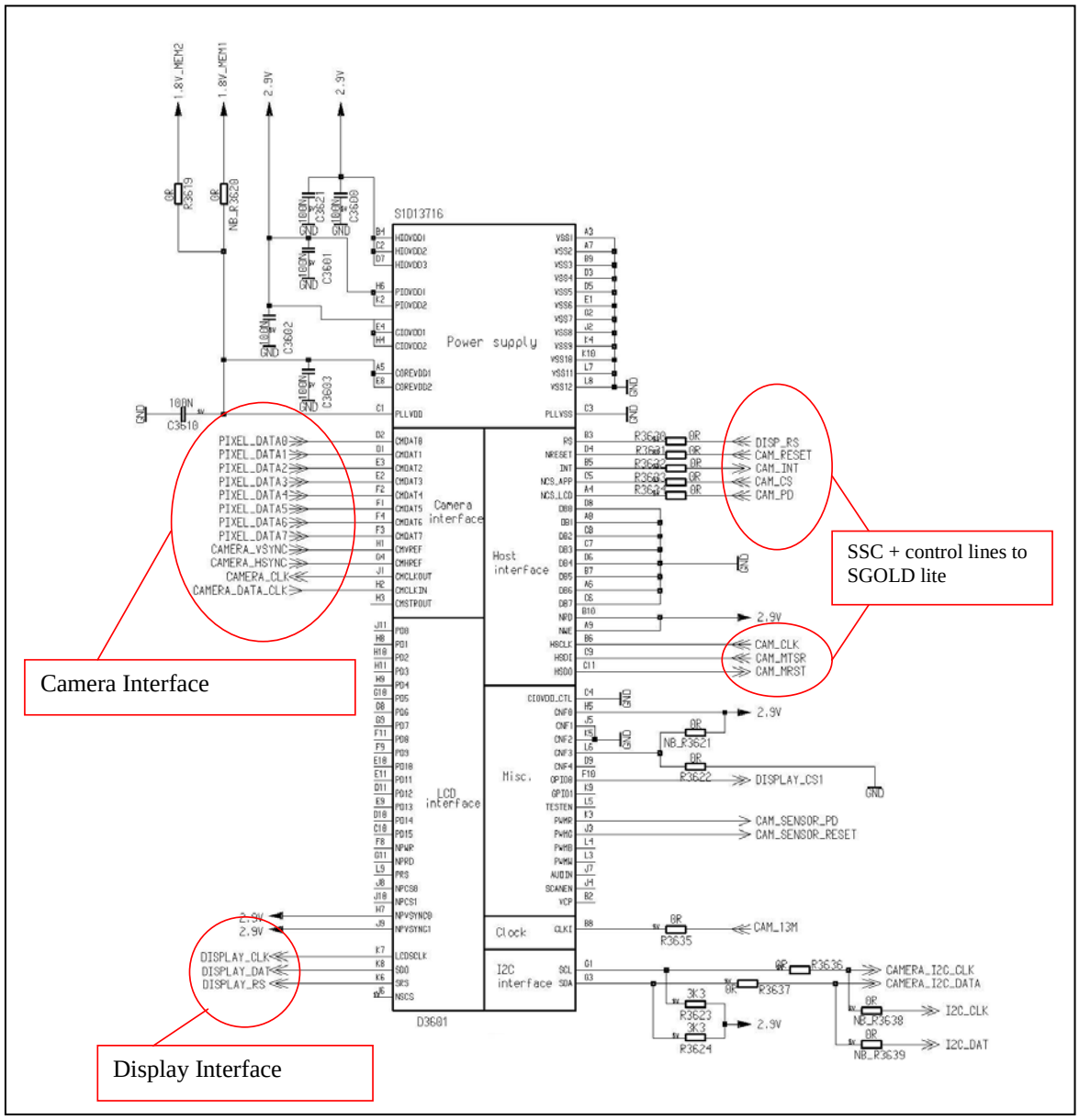
In this mode the S1D13716 is transparent regarding the display. The S-GOLDlite communicates “directly” with the display.

b) Camera View Mode:

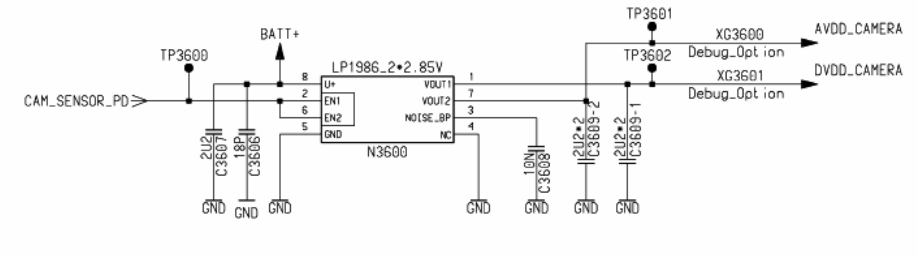
In this mode the S1D13716 transfers the picture – data from the camera directly to the display. A resizing and compressing engine is available to reduce the data amount to the display. So the preview can be done without using the SGOD performance.

c) Camera Capture Mode:

In this mode the picture – data from the camera is sent to the SGOLD. There are resizing and compressing engines available to reduce the data-stream to the SGOLD-lite



Voltage supply for Camera Asic



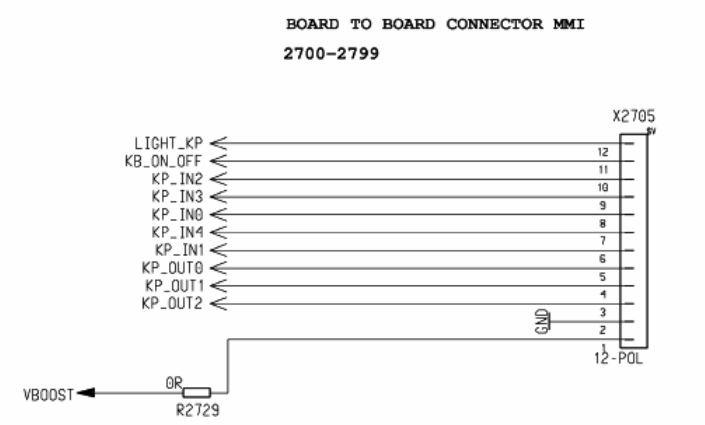
12 Display Modules

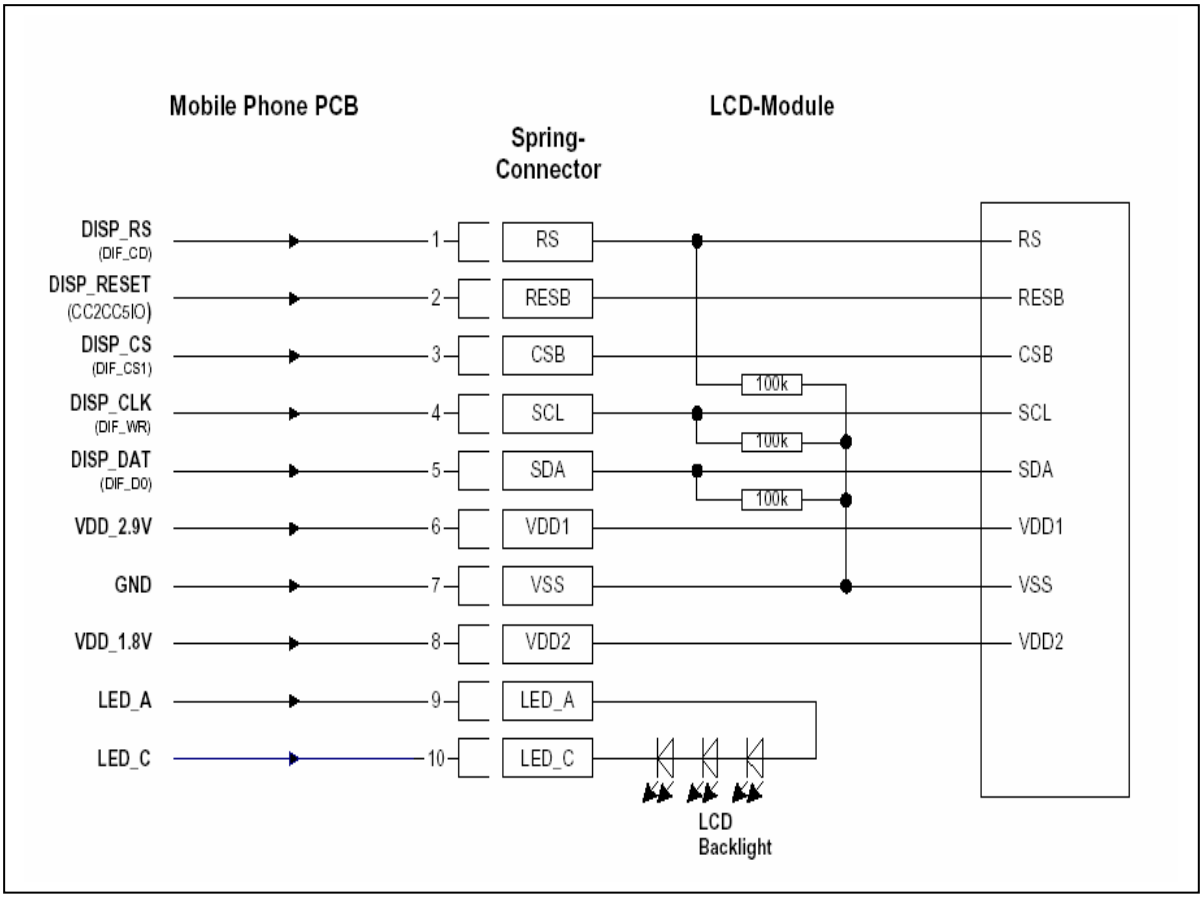
12.1 Display C65, C70, C72

The display has a resolution of 130x130 pixels with a colour depth of 65536 colours. It contains an passive matrix panel (CSTN) where the colours are generated by red, green and blue colour filters and a plastic housing. For the display two different sources are used , which will be distinguished by the software via different code resistor values. Both modules use different LCD-controllers. The controller is directly mounted on the panel of the display (COG). In order to guarantee a very efficient illumination the white LEDs are mounted on a flexfoil inside the module. In addition, all passive components necessary to drive an LCD are also assembled on this flexfoil. The software can detect the displays automatically due to the hardware coding. Thus, the only interconnections to the Siemens PCB are the data lines and the power supply lines of the controller and the white LEDs. The interface is realized by spring connector with 10 interconnections which is assembled on the Siemens PCB.

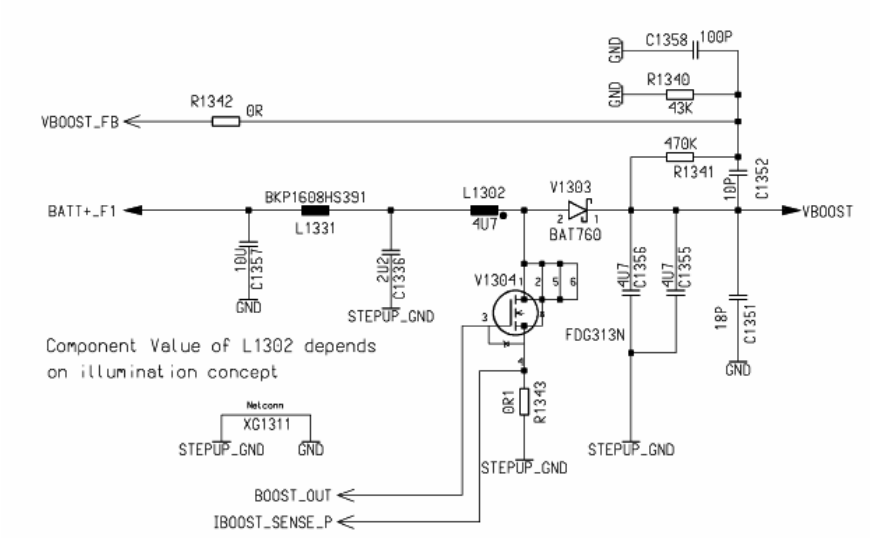
12.2 Display CX70

The display has a resolution of 132x176 pixels with a color depth of 65536 colors. It contains an active-matrix panel where the colors are generated by red, green and blue color filters and a plastic housing. For the display two different sources are used, which will be distinguished by the software via different code resistor values. Both modules use different LCD-controllers. The controller is directly mounted on the panel of the display. In order to guarantee a very efficient illumination the white LEDs are mounted on a flexfoil inside the module. In addition, all passive components necessary to drive an LCD are also assembled on this flexfoil. The software can detect the displays automatically due to the hardware coding. Thus, the only interconnections to the Siemens PCB are the data lines and the power supply lines of the controller and the white LEDs. The interface is realized by spring connector with 10 interconnections which is assembled on the Siemens PCB.


BOARD TO BOARD CONNECTOR MMI
2700-2799
X2705
LIGHT_KP
KB_ON_OFF
KP_IN2
KP_IN3
KP_IN0
KP_IN4
KP_IN1
KP_OUT0
KP_OUT1
KP_OUT2
GND
12-POL
VBOOST
0R
R2729


Mobile Phone PCB
Spring-
Connector
LCD-Module
DISP_RS
(DIF_CD)
DISP_RESET
(CC2CC5IO)
DISP_CS
(DIF_CS1)
DISP_CLK
(DIF_WR)
DISP_DAT
(DIF_D0)
VDD_2.9V
GND
VDD_1.8V
LED_A
LED_C
1
2
3
4
5
6
7
8
9
10
RS
RESB
CSB
SCL
SDA
VDD1
VSS
VDD2
LED_A
LED_C
100k
100k
100k
RS
RESB
CSB
SCL
SDA
VDD1
VSS
VDD2
LCD
Backlight

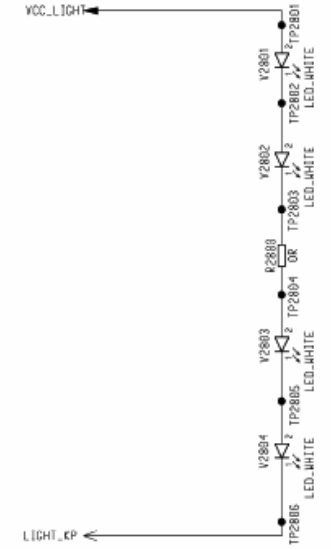
The display controller is being driven with a supply voltage of VDD1_2.9V = 2.90 V and VDD2_1.8V=1.8 V. The 3 white side-shooter LEDs are driven in serial. The maximum current is 15mA. The voltage for the 3 LEDs is VDD_Boost.



13 Illumination

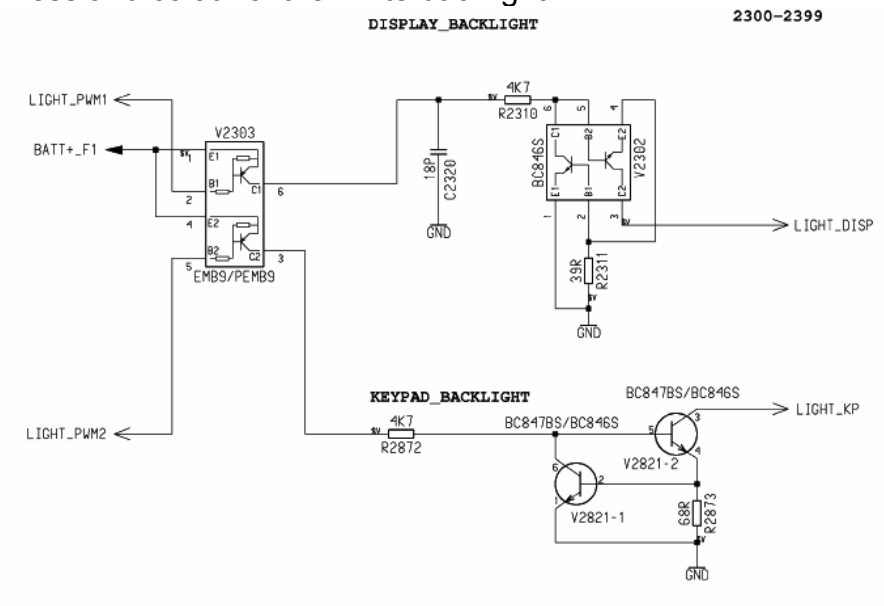
a) Keyboard

The LED´s will be mounted on separate MMI-PCB. The illumination of the keypad will be done via high-brightness LEDs (colour: white, type: top-shooter, driven by 7.5 mA / LED). The LEDs will be driven by one current source with a maximum current of 15 mA. The 6 LEDs are divided in two groups with 3 LEDs in serial.



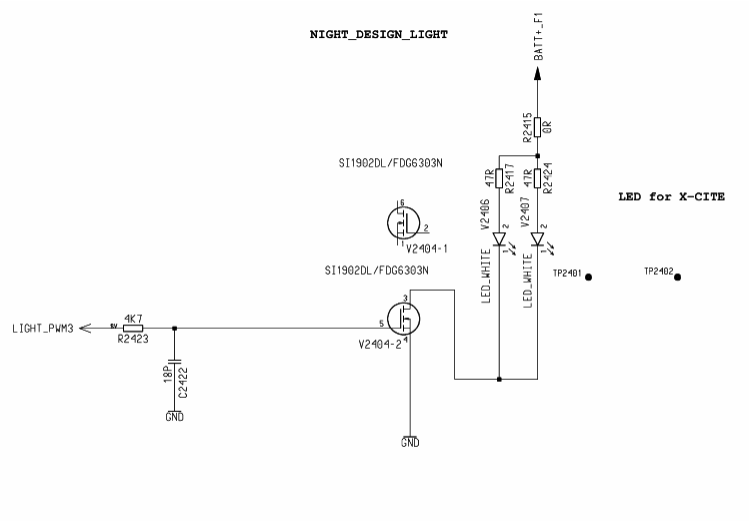
b) Display

The 3 serial LEDs for the display are supplied by one constant current sources, to ensure the same brigthness and colour of the white backlight.



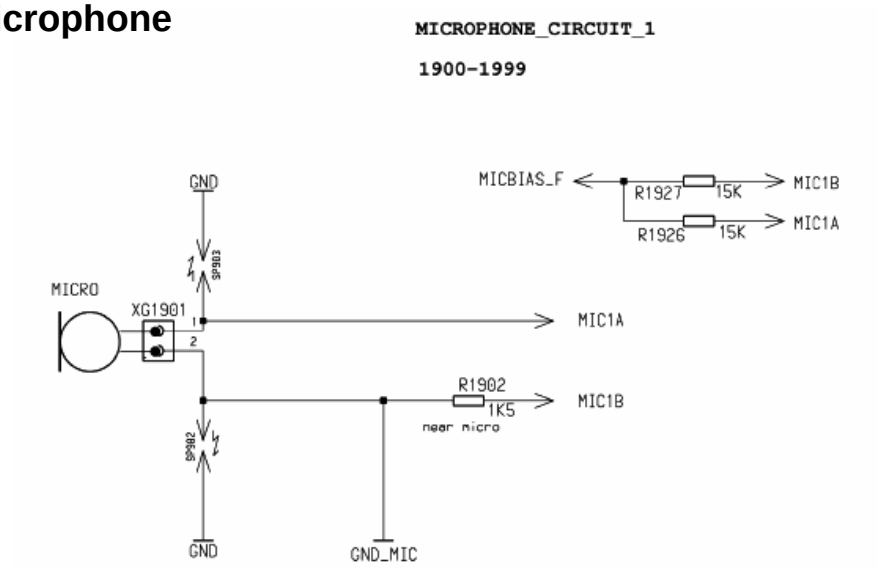
c) Dynamic Light only CX70

The 2 white LEDs for the dynamic light are directly contacted to the battery pack. One transistor is used for both LEDs to control the brightness. Also a PWM is necessary to prevent a damage of the LEDs when the battery pack is fully charged.



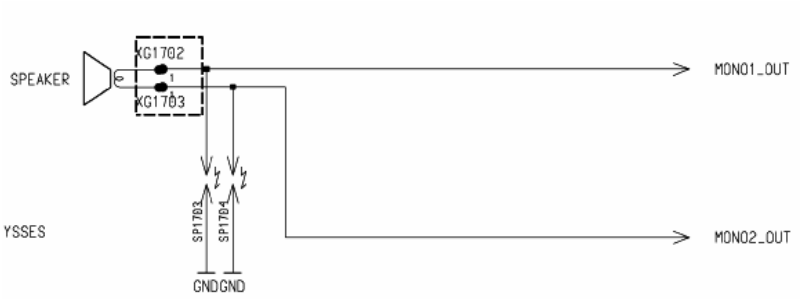
14 Interfaces

14.1 Microphone



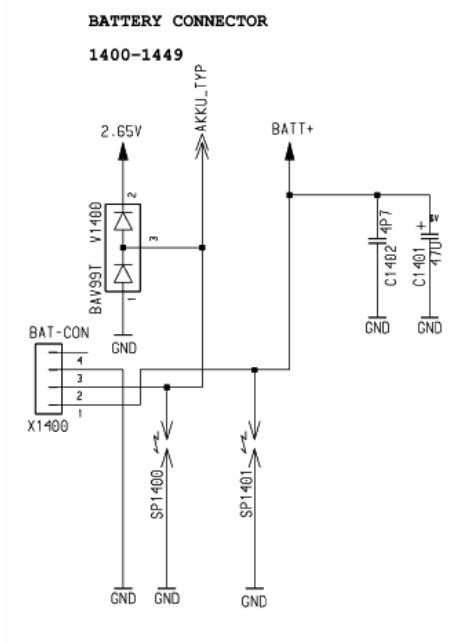
Pin	Name	IN/OUT	Remarks
1	MIC1A	O	Microphone power supply. The same line carries the low frequency speech signal.
2	MIC1B		GND_MIC

14.2 Loudspeaker



Pin	Name	IN/OUT	Remarks
1	MONO1_OUT	O	1st connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. EPP1 builds together with EPN1 the differential output to drive the multifunctional “earpiece” (earpiece, ringer, handsfree function).
2	MONO2_OUT	O	2nd connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation.

14.3 Battery

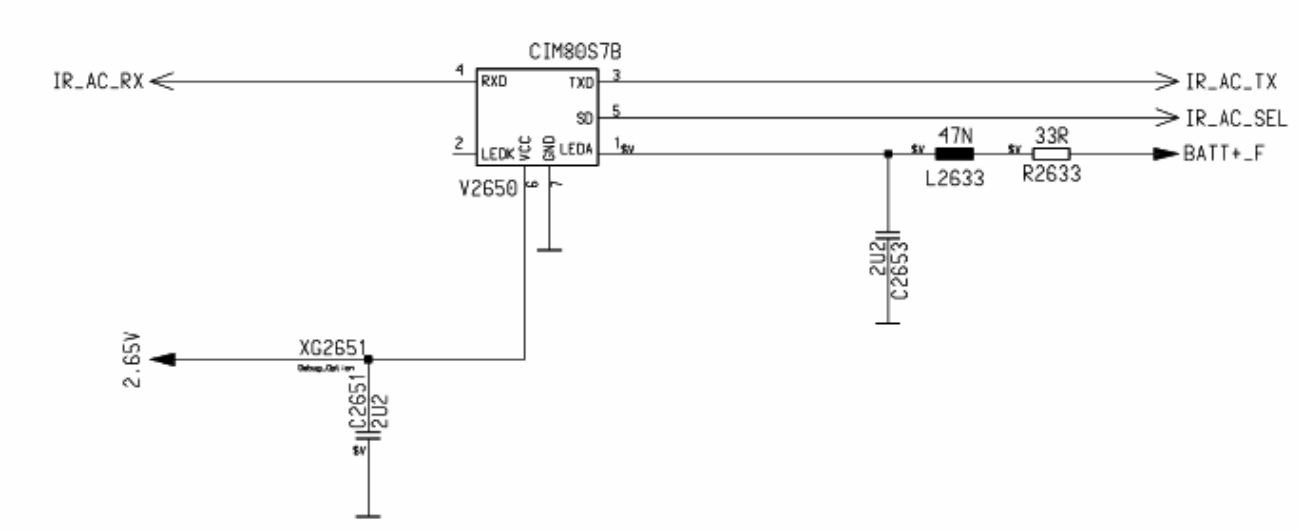


Pin	Name	Level	Remarks
1	GND	-	Ground
2	AKKU_TYP	0V...2.65V	Recognition of battery/supplier
3	BATT+	3 V... 4.5V	Positive battery pole

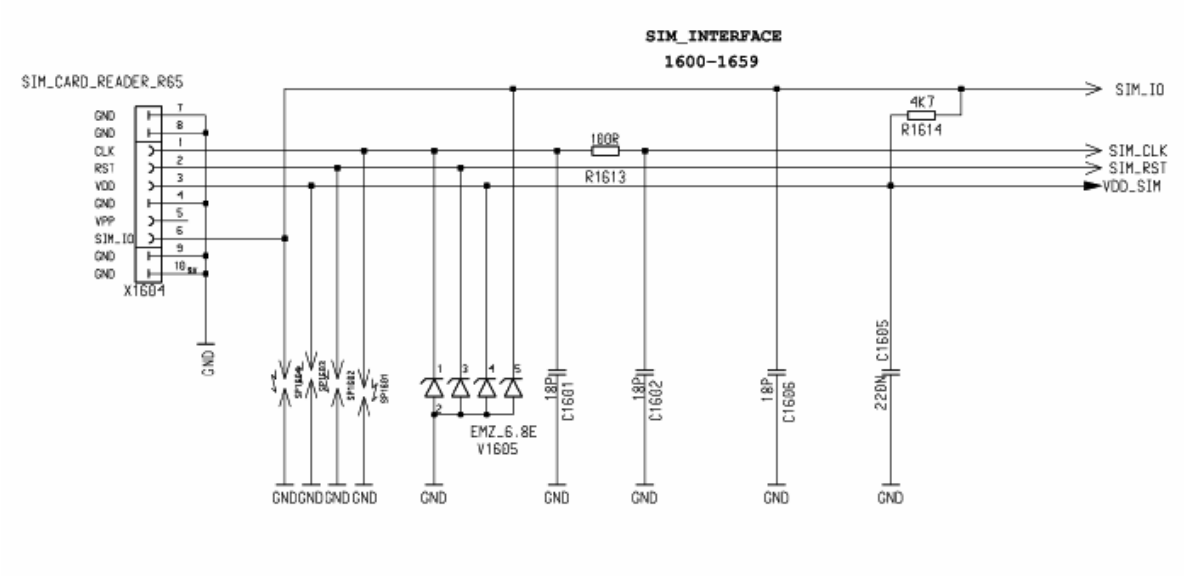
14.4 IRDA

A Low-Power infrared data interface, compatible to ”IrDA - Infrared Data Association; Serial Infrared Physical Layer Specification, Version 1.3”, supporting transmission rates up to 115.2kbps (Slow IrDA) will be provided. As a Low-Power-Device, the infrared data interface has a transmission range of at least:

- 20cm to other Low-Power-Devices and
- 30cm to Standard-Devices



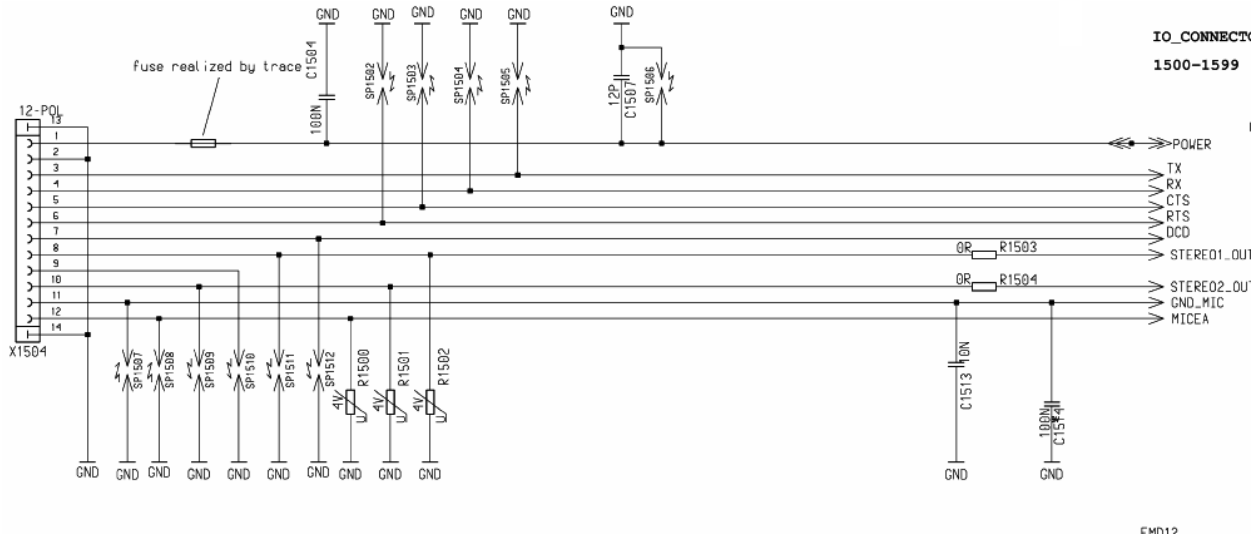
14.5 Interface SIM Module



Pin Name	IN/OUT	Remarks
SIM_CLK	O	Pulse for chipcard. The chipcard is controlled directly from the SGOLD+.
SIM_RST	O	Reset for chipcard
SIM_IO	I	Data pin for chipcard; 4,7 kΩ pull up at the VDD_SIM pin
	O	
VDD_SIM	O	Switchable power supply for chipcard; 220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes.

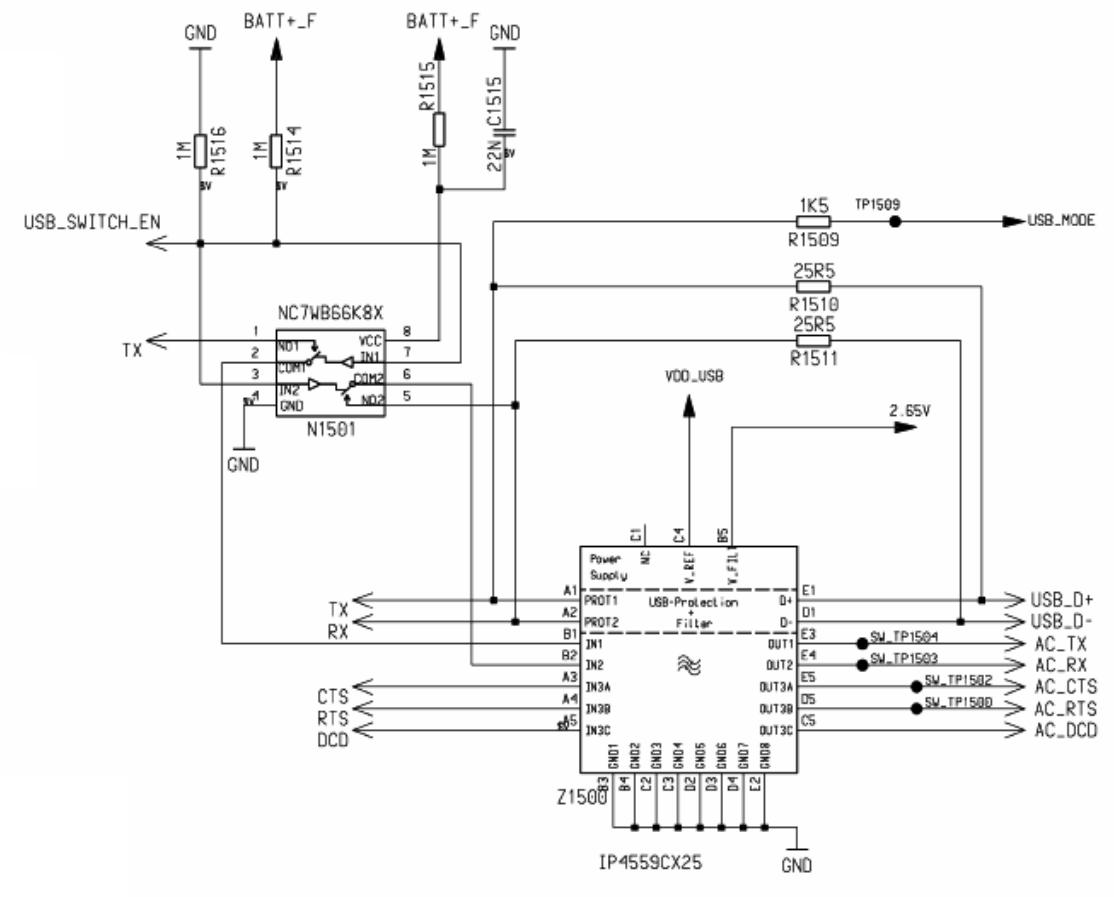
14.6 IO Connector with ESD protection

14.6.1 IO Connector – New Slim Lumberg



Pin	Name	IN/OUT	Notes
1	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
2	GND		
3	TX/D+	OI/O	Serial interface USB-interface full-speed 12Mbit/s
4	RX/D-	I	Serial interface USB-interface full-speed 12Mbit/s
5	DATA/CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
6	RTS	I/O	Use as RTS in data-operation.
7	CLK/DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
8	STEREO1_OUT	Analog O	driving ext. headset STEREO1_OUT and STEREO2_OUT differential mode
9	GND		
10	STEREO2_OUT	Analog O	driving ext. right to PHANTOM_BUF_OUT with mono-headset STEREO1_OUT and STEREO2_OUT differential mode
11	GND_MIC	Analog I	for ext. microphone
12	MICEA_AC	Analog I	External microphone

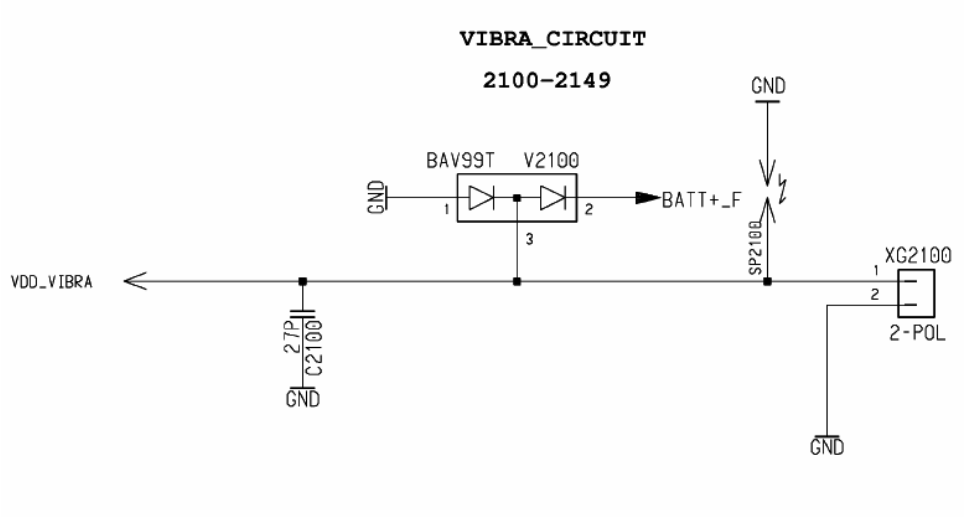
14.6.2 ESD Protection with EMI filter



The Z1500 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z1500 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages

14.7 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts



Pin	Name	IN/OUT	Remarks
1	VDD_VIBRA		Vbatt will be switched by PWM-signal with internal FET to VDD_Vibra in Asic
2	GND		

15 Keyboard

The keyboard is connected via the lines KPOUT0 – KPOUT3 and KPIN0 – KPIN4 with the SGOLDLITE. KB_ON_OFF is used for the ON/OFF switch. KP_INO is used for the side keys. KPIN0 – KPIN4 and KPOUT3 is used for the joystick.