# A55/C55 Hitachi

# Level 2.5e

# Repair Documentation

V 1.20

| Version | Date | Department | Notes to change |
|---|---|---|---|
| V 0.95 | 28.08.2002 | ICM MP CCQ S T | New document |
| V 1.00 | 24.10.2002 | ICM MP CCQ GRM | Modified document |
| V 1.10 | 17.02.2003 | ICM MP CCQ GRM | Modified document |
| V 1.20 | 30.04.2003 | ICM MP CCQ GRM | Modified document |

# Table of Contents:



# 1 List of available level 2,5e parts A55/C55

| ID-No | Type | Board | Name, Location | Part-No. |
|---|---|---|---|---|
| D150 | VCO | HIT | Transmitter_VCO | L36820-L6097-D670 |
| D1600 | VCO | IFX | Transmitter_VCO | L36820-L6109-D670 |
| D171 | IC | HIT/IFX | Egold+ | L36810-G6149-D670 |
| D1740 | Filter | IFX | Ant_Switch_Diplexer | L36197-F5006-F936 |
| D1785 | IC | IFX | Transceiver IC | L36197-F5011-F334 |
| D361 | IC | HIT/IFX | ASIC | L36145-J4682-Y43 |
| D800 | IC | HIT | Transceiver IC | L36820-L6105-D670 |
| D920 | IC | HIT | PA_Comperator | L36820-L6133-D670 |
| R1507 | Resistor | IFX | Temp_Resistor | L36120-F4223-H |
| R959 | Resistor | HIT | Temp_Resistor | L36120-F4223-H |
| V1500 | Diode | IFX | Capa_Diode | L36840-D61-D670 |
| V151 | Diode | HIT/IFX | Diode_KB7 | L36840-D5062-D670 |
| V181 | Diode | HIT/IFX | Diode_Battery_Interface | L36702-A1051 |
| V211 | Transistor | HIT/IFX | Tran._Vibra | L36830-C1097-D670 |
| V220 | Diode | HIT/IFX | Diode_Vibra | L36851-Z9105-Z981 |
| V222 | Transistor | HIT/IFX | Trans_Light_ | L36830-C1112-D670 |
| V223 | Transistor | HIT | Trans_Light_ | L36840-C4004-D670 |
| V361 | Transistor | HIT/IFX | Tran._Charge | L36830-C1110-D670 |
| V850 | Transistor | HIT | Tran._VCO_Switch | L36820-C6047-D670 |
| V920 | Diode | HIT | Feedback_Diode | L36840-D5049-D670 |
| V921 | Transistor | HIT | Tran._PA_Switch | L36820-C6047-D670 |
| V950 | Transistor | HIT | Tran._26MHz_Ampl. | L36840-C4049-D670 |
| V951 | Diode | HIT | Capa_Diode | L36840-D61-D670 |
| Z1500 | Quartz | IFX | Oszillator_26MHz | L36145-F260-Y17 |
| Z1600 | Filter | IFX | Transmitter_Filter | L36145-K280-Y242 |
| Z1700 | IC | IFX | Power_Amplifier | L36197-F5005-F487 |
| Z171 | Quartz | HIT/IFX | Quarz/Egold | L36145-F102-Y8 |
| Z211 | Filter | HIT/IFX | Logic/IO_Interface | L36197-F5000-F116 |
| Z850 | VCO | HIT | 1LO_VCO | L36145-G100-Y96 |
| Z851 | Filter | HIT | Filter_BALUN | L36145-K260-Y41 |
| Z880 | IC | HIT | Ant_Switch_Diplexer | L36145-K280-Y257 |
| Z900 | IC | HIT | Power_Amplifier | L36851-Z2002-A59 |
| Z950 | Quartz | HIT | Oszillator_26MHz | L36145-F260-Y17 |

# 2 Required Equipment for Level 2,5e

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector
- Troubleshooting Frame A55/C55 (F30032-P209-A1)
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

*Reference:* Equipment recommendation V1.2
(downloadable from the technical support page)

# 3 Required Software for Level 2,5e A55/C55

- Windows NT Version4
- Winsui version1.38 or higher
- Software for GSM-Tester ( Cats(Acterna/Wiltek) or CMU-GO(Rohde&Schwarz) )
- Software for reference oscillator adjustment
- Internet unblocking solution
- Dongle driver for USB-Dongle if used with WIN NT4

# 4 Radio Part

The radio part of the A55/C55, is using a Hitachi and an Infineon RF chip-set. This manual covers the Hitachi chip-set. For Infineon there is an additional manual available.

The radio part is designed for Dual Band operation, covering EEGSM900 as well as GSM 1800 frequencies, and can be divided into 4 Blocks.

- -Power supply for RF-Part
- -Transmitter
- -Receiver
- -Synthesizer,

The RF-Part has it´s own power supply realised by a voltage regulator which is located
inside the ASIC. The voltages for the logic part are generated by the Power-Supply ASIC too.

The transmitter part converts the I/Q base band signals supplied by the logic (EGOLD+) into RF-signals with characteristics as defined in the GSM recommendation (www.etsi.org) After amplification by a power Amplifier the signal is radiated via the internal or external antenna.

The receiver part converts the received GMSK signal supplied by the antenna into IQ base band signals which are further processed by the logic (EGOLD+).

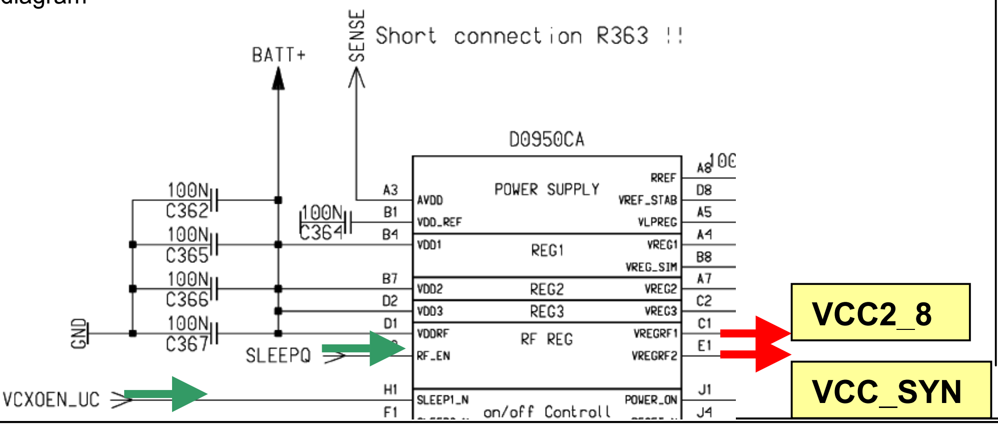
The synthesizer generates the required frequencies for the transmitter and receiver. A 26MHz oscillator is acting as a reference frequency.

Restrictions:
The mobile phone can never transmit and receive in both bands simultaneously. Only the monitor time slot can be selected independently of the frequency band. Transmitter and receiver can of course never operated simultaneously.

## 4.1 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D361.(see chapter 5.2)
It generates the required 2,8V "RF-Voltages" named VCC2_8 and VCC_SYN . The voltage regulator is activated as well as deactivated via SLEEPQ (TDMA-Timer H16) and VCXOEN_UC (Miscellaneous R6) provided by the EGOLD+. The temporary deactivation is used to extend the stand by time.

Circuit diagram



## 4.2 Frequency generation

### 4.2.1 Synthesizer: The discrete VCXO (26MHz)

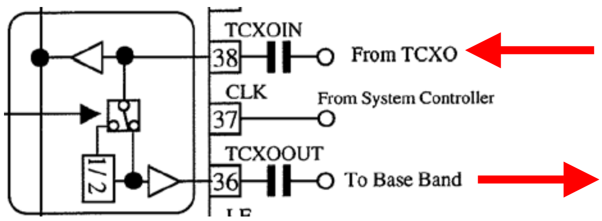
The A55/C55 mobile is using a reference frequency of 26MHz for the Hitachi chip set. The generation of the 26MHz signal is done via a discrete “Colpitts” VCXO. This oscillator consists mainly of:

| | |
|---|---|
| A 26MHz crystal | Z950 |
| An oscillator switch | V950 |
| A capacity diode | V951 |

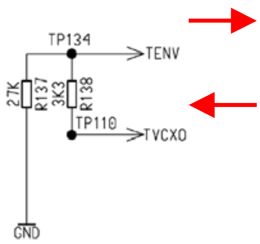
TP (test point) of the 26MHz signal is the TP 1501

The oscillator output signal 26MHz_RF is directly connected to the BRIGHT IC (pin 38) to be used as reference frequency inside the Bright (PLL). The signal leaves the Bright IC as BB_SIN26M at pin 36 to be further used from the EGOLD+ (D100 (**functional T3**)).

**Bright 4**

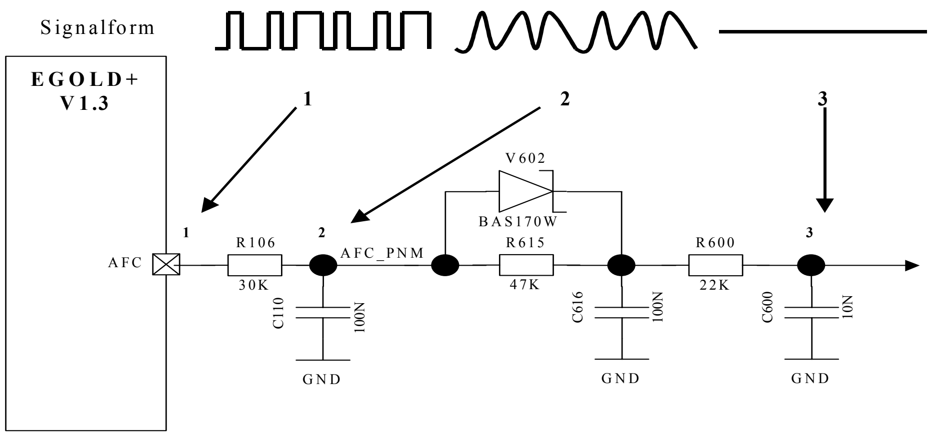



To compensate frequency drifts (e.g. caused by temperature) the oscillator frequency is controlled by the (AFC) signal, generated through the internal EGOLD+ (D100 (**functional U5**)) PLL via the capacity diode V951. Reference for the “EGOLD-PLL” is the base station frequency. To compensate a temperature caused frequency drift, the temperature-depending resistor R959 is placed near the VCXO to measure the temperature. The measurement result TVCXO is reported to the EGOLD+(**Analog Interface P3**) via R138 as the signal TENV.

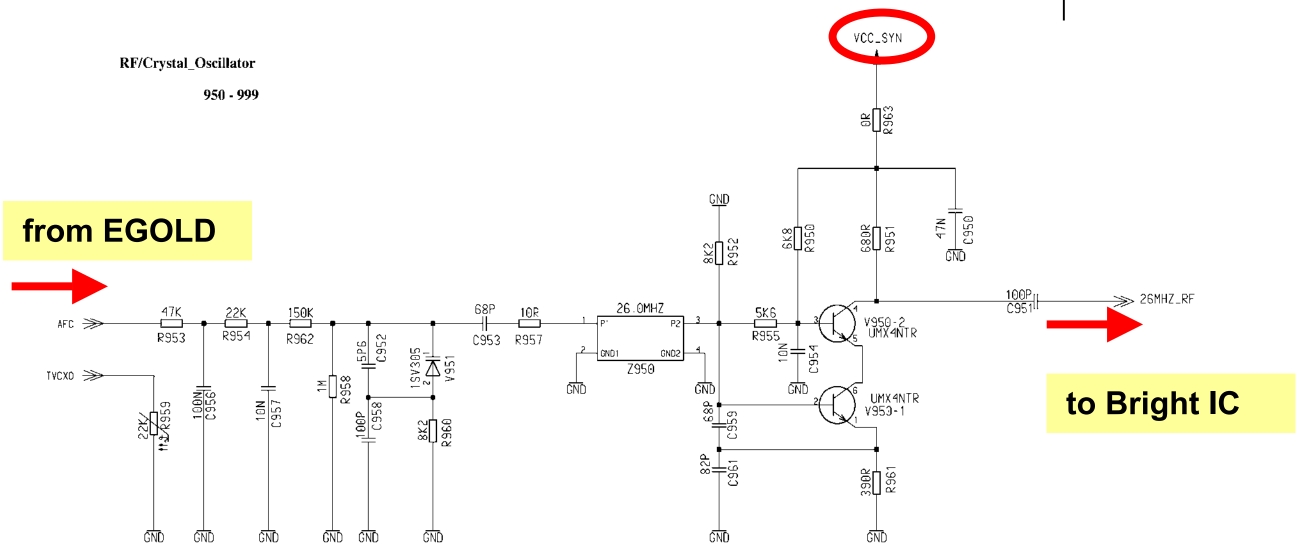



The required voltage VCC_SYN is provided by the ASCI D361

**Waveform of the AFC_PNM signal from EGOLD+ to Oscillator**



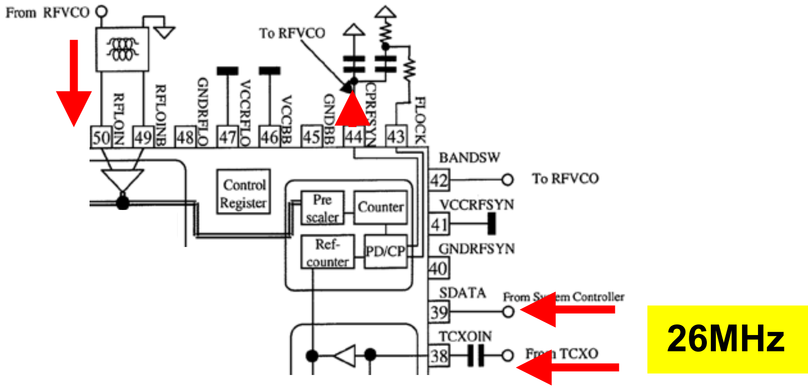

**Circuit diagram**



### 4.2.2 Synthesizer: LO1

The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. To do so, a control voltage for the LO1 is used. Gained by a comparator. (located inside the Transceiver (Bright -IC). This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the EGOLD+, according to the network channel requirements.




The first local oscillator (LO1) consists of the PLL inside the Bright (D800), an external loop filter and the VCO (Z850) module. This LO1 circuit generates frequencies from

3700-3980 MHz for EEGSM900
3580-3760 MHz for GSM1800

**Formula to calculate the TX frequencies:**

EEGSM900

| | |
|---|---|
| Channel: 975...1023/76...92 | = (Channel freq. + 82MHz) * 4 |
| Channel: 0…75/93…124 | = (Channel freq. + 80MHz) * 4 |

GSM1800

| | |
|---|---|
| Channel: 512...661 | = (Channel freq. + 80MHz) * 2 |
| Channel: 662…885 | = (Channel freq. + 82MHz) * 2 |

**Formula to calculate the RX frequencies:**

EEGSM900 = Channel freq. * 4 GSM1800 = Channel freq. * 2

The VCO (Z850) is switched on by the EGOLD+ signal PLLON (TDMA-Timer F16) via V850 and therefore supplied with VCC2_8. The VCO guarantees by using the control voltage at pin5 a coverage of the EEGSM900, GSM1800 frequency band and the frequency stability. The Bright gained control voltage passes on the way to the VCO a discreet loop filter (typical value from 0,5 – 2,1V). The channel programming of the PLL happens via the EGOLD+ signals RFDATA; RFCLK; RFSTR. (RF Control J15, J16, J17). If the Bright IC gets via the same signals a GSM1800 channel information, the VCO is switched to this frequency by Pin 42 Bright (Pin 3 VCO).

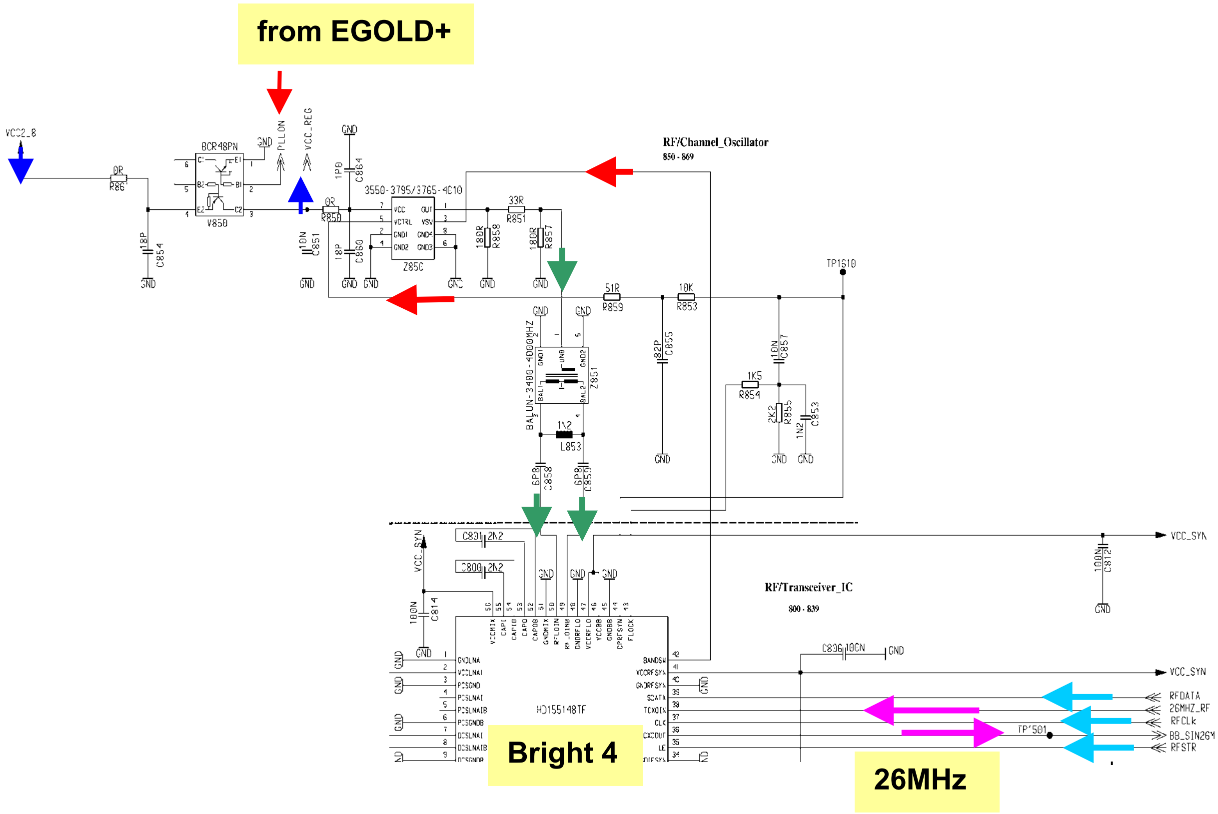
| | | |
|---|---|---|
| For GSM900 | - RX | = "low signal" for channel 975-49 |
| | | = "high signal" for channel 50-124 |
| | - TX | = "high signal" for all channels |
| For GSM1800 | - RX | = "low signal" for all channels |
| | - TX | = "low signal" for all channels |

The VCO output signal passes the "Balun" transformer (**Z851**) with insertion losses of ~ 2dB to arrive at the Bright IC.

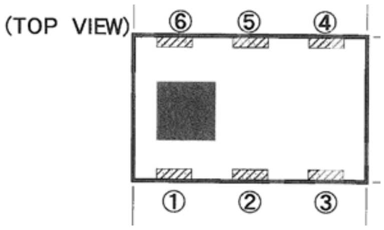
The required voltage VCC8_8 is provided by the ASIC D361

Circuit diagram



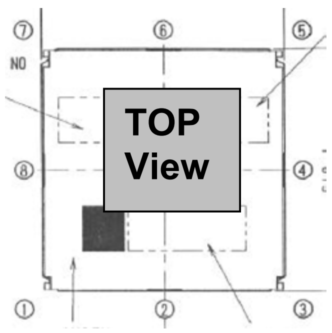

**Balun transformer**




PIN FUNCTION

①Unbalanced Port
②GND
③Balanced Port1
④Balanced Port2
⑤GND
⑥N. C

**VCO**




| TERMINAL NO. | CONTENTS |
|---|---|
| 1 | OUT |
| 2 | GND |
| 3 | SW |
| 4 | GND |
| 5 | VCTL |
| 6 | GND |
| 7 | VCC |
| 8 | GND |

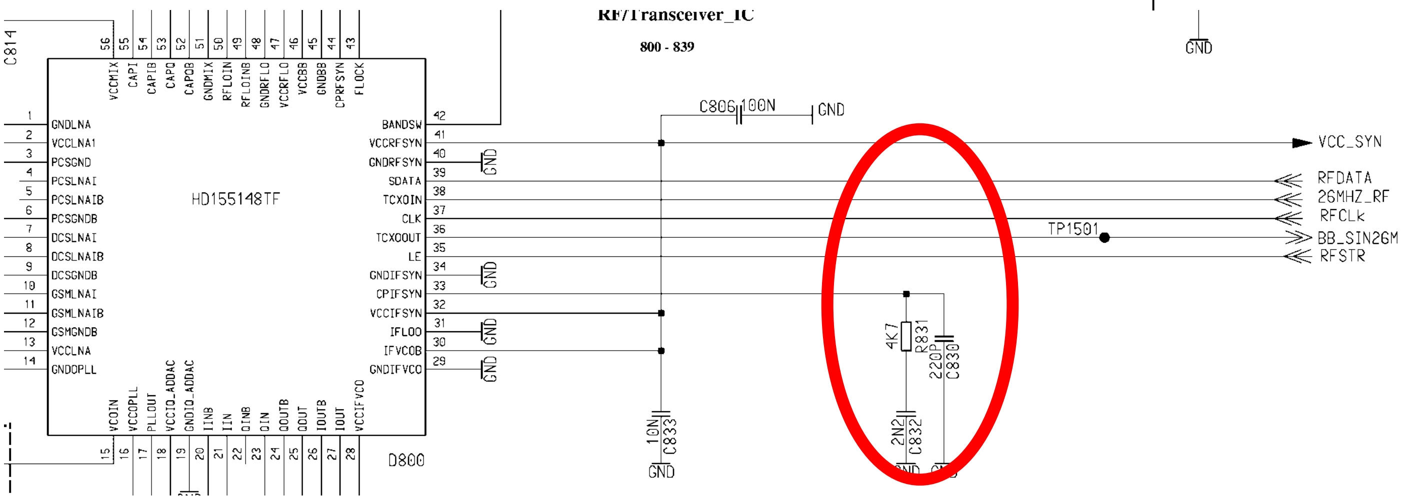
  

### 4.2.3 Synthesizer: LO2

The second local oscillator is required for transmitter operations only. It consists of a PLL and a VCO which are integrated inside the Bright 4, and an external second order loopfilter (R831; C830; C832). Before the VCO generated 640 or 656MHz signal arrives at the modulator, it is divided by 8. So the resulting frequency after the IQ modulator is 80/82MHz (dependent on the channel and band). Programming of the LO2 PLL is done in the same way as described at the LO1 the tree-wire-bus (EGOLD+ signals RFDATA; RFCLK; RFSTR. (RF Control J15, J16, J17) is used. To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2nd PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

The required voltage VCC_SYN is provided by the ASIC D361

Circuit diagram

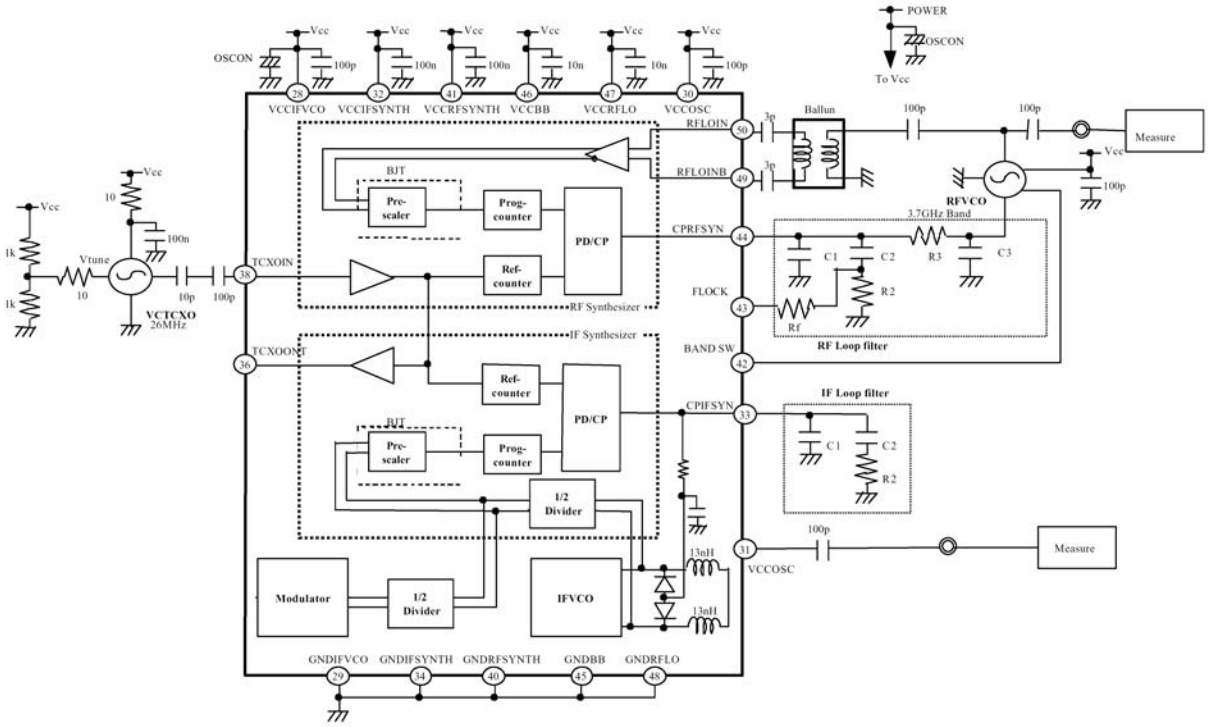



Loop-filter LO2

### 4.2.4 Synthesizer: PLL

PLL as a part of the BRIGHT IC

Blockdiagram



## 4.3 Antenna switch (electrical/mechanical only C55)

Internal/External <> GSM1800/900 <> Receiver/Transmitter

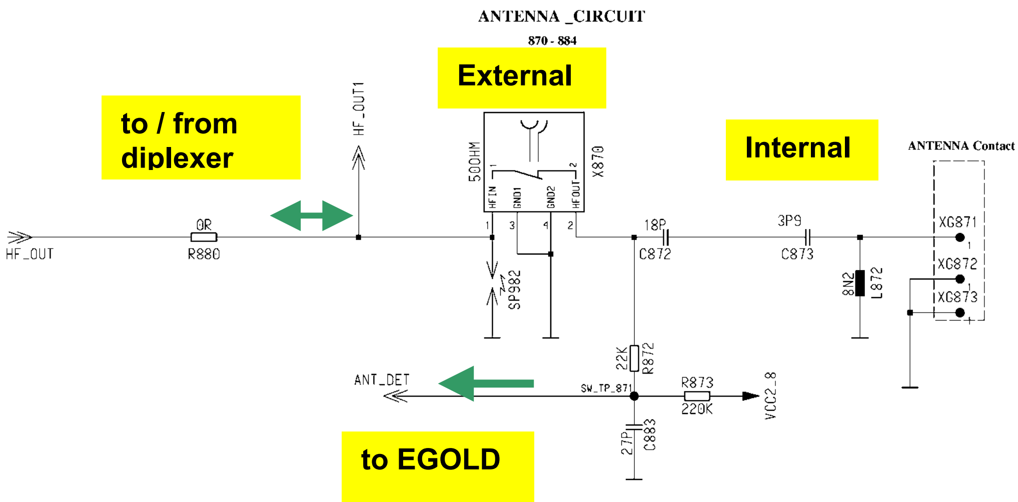
The C55 mobile has two antenna switches. A55 has no external antenna connector/mechanical antenna switch.

a) The mechanical antenna switch for the differentiation between the internal and external antenna

b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals.
To activate the correct settings of this diplexer, the EGOLD+ signals RF_SW and TXON_GSM are required

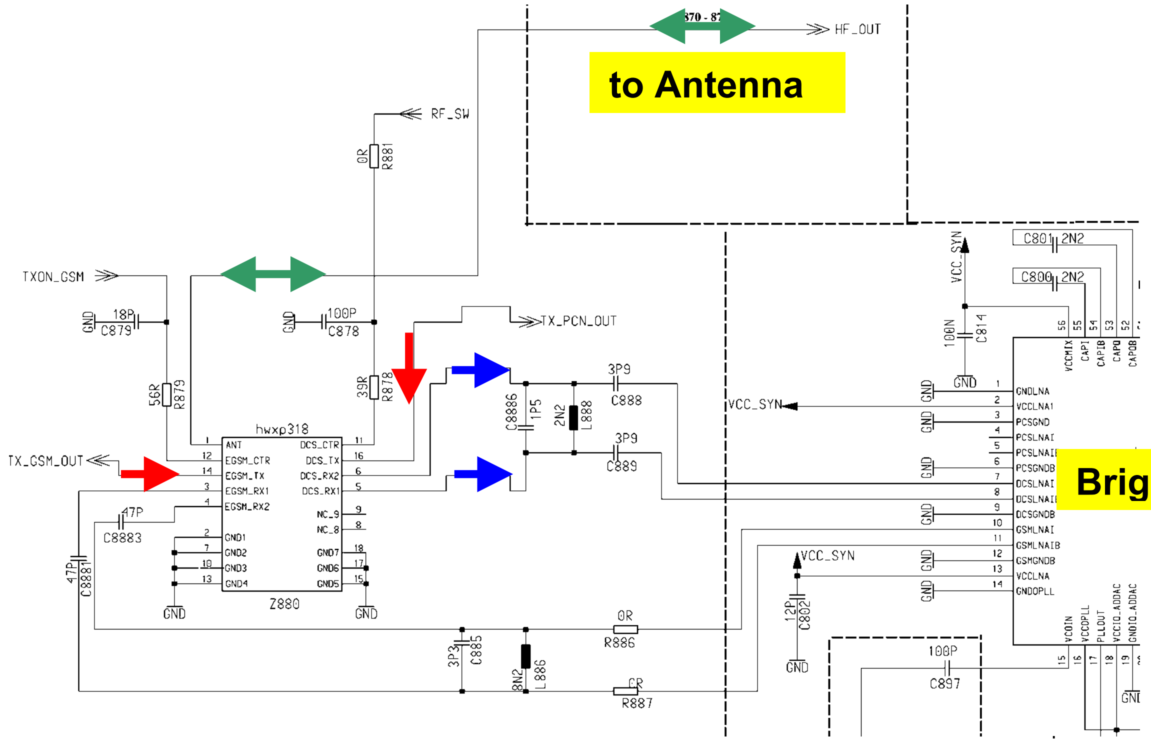
As a new feature the A55/C55 has an integrated "SAR detection" circuit. This circuit is used to decide if the internal antenna or an external antenna is used. The goal is, to reduce the transmit power when the internal antenna is used and the mobile is held very close to the body. On the other hand, the mobile can send with more power, if the external antenna is used. This distinction is done by the SAR detection circuit which consists of the voltage divider R872 and R873. The ANT_DET output provides a high level when the external antenna is used. ANT_DET (Serial Interface L16) is connected to the EGOLD+

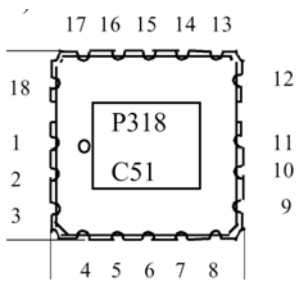
a) Internal/External antenna switch



b) The electrical antenna switch




**Z880**
**Top View**

| | | | |
|---|---|---|---|
| 1 | ANT | 10 | GND |
| 2 | GND | 11 | Vc(DCS) |
| 3 | EGSM-Rx1 | 12 | Vc(EGSM) |
| 4 | EGSM-Rx2 | 13 | GND |
| 5 | DCS-Rx1 | 14 | EGSM-Tx |
| 6 | DCS-Rx2 | 15 | GND |
| 7 | GND | 16 | DCS-Tx |
| 8 | NC | 17 | GND |
| 9 | NC | 18 | GND |

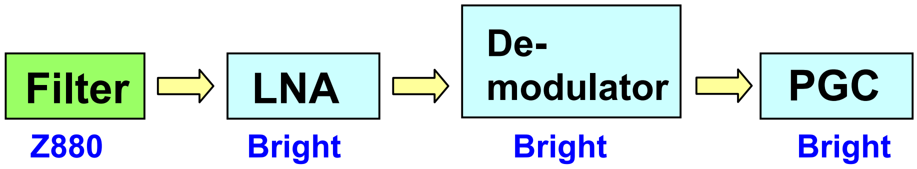
| | | EGSM | | DCS | |
|---|---|---|---|---|---|
| | | Rx | Tx | Rx | Tx |
| Vc (EGSM) | 0V | on | off | - | - |
| | 2.5V (10mA) | off | on | - | - |
| Vc (DCS) | 0V | - | - | on | off |
| | 2.5V (10mA) | - | - | off | on |

## 4.4 Receiver

### 4.4.1 Receiver: EGSM900/1800 –Filter to Demodulator

From the antenna switch, up to the demodulator the received signal passes the following blocks to get the demodulated baseband signals for the EGOLD+:




Filter: The EGSM900 and GSM 1800 filters are located inside the frontend module. The Filter are centred to a frequency of 942,5MHz for EEGSM900 and 1847,5MHz for GSM1800. The symmetrical filter output is matched via LC-Combinations to the LNA input of the BRIGHT (D800)

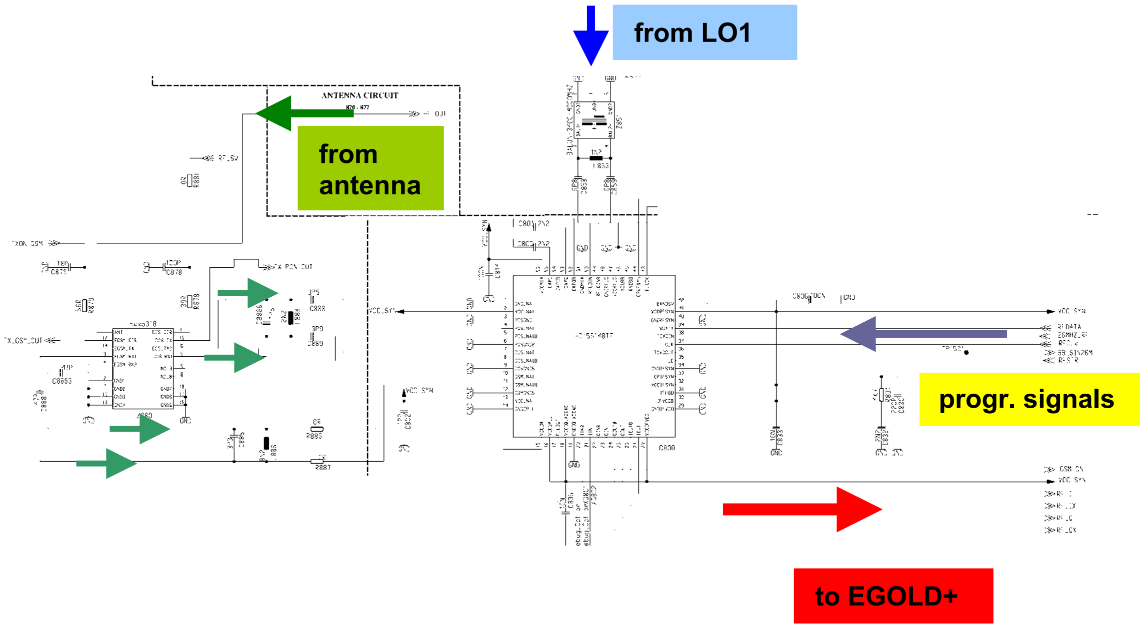
LNA: The 2 LNA´s (EGSM900/1800) are located inside the BRIGHT and are able to perform an amplification of ~ 20dB. The LNA can be switched in HIGH (On) and LOW (Off) mode and is controlled by the Bright depending on EGOLD+ information.

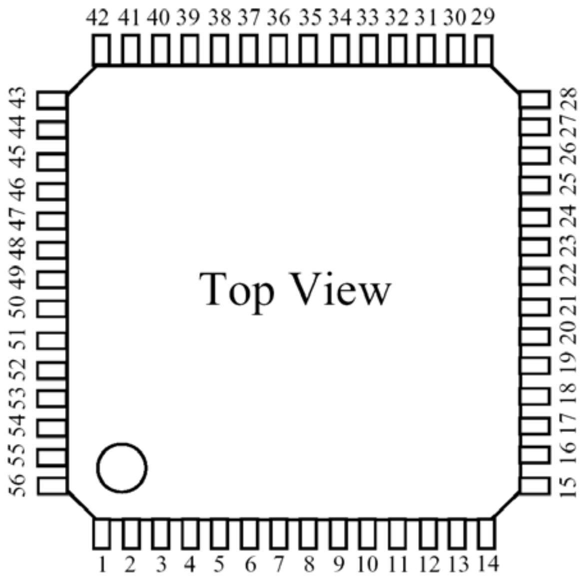
Demodulator: The Bright IC performs a direct demodulation of the received GSM signals. To do so the LO1 is required. The channel depending LO1 frequencies for 1800MHz band are divided by 2 and by 4 for 900MHz band, Bright internally.

PGC: After demodulation the “I” and “Q” signals are amplified by the PGC-Amplifier the “I” and the “Q” path are amplified independently from each other. The performance of this PGC is 80dB (-26 up to 54dB), switchable in steps of 2dB. The control is realised through the EGOLD+ signals (RFDATA; RFCLK; RFSTR.(RF Control J15, J16, J17). After passing a Bright internal switch (necessary because of the double using of RX and TX lines), the signals are ready for further processing through the EGAIM (part of the EGOLD+) The post-switched logic measures the level of the demodulated baseband signal an regulates the level to a defined value by varying the PGA-Amplification and switching the appropriate LNA gains

The required voltage VCC_SYN is provided by the ASIC D361

Circuit diagram

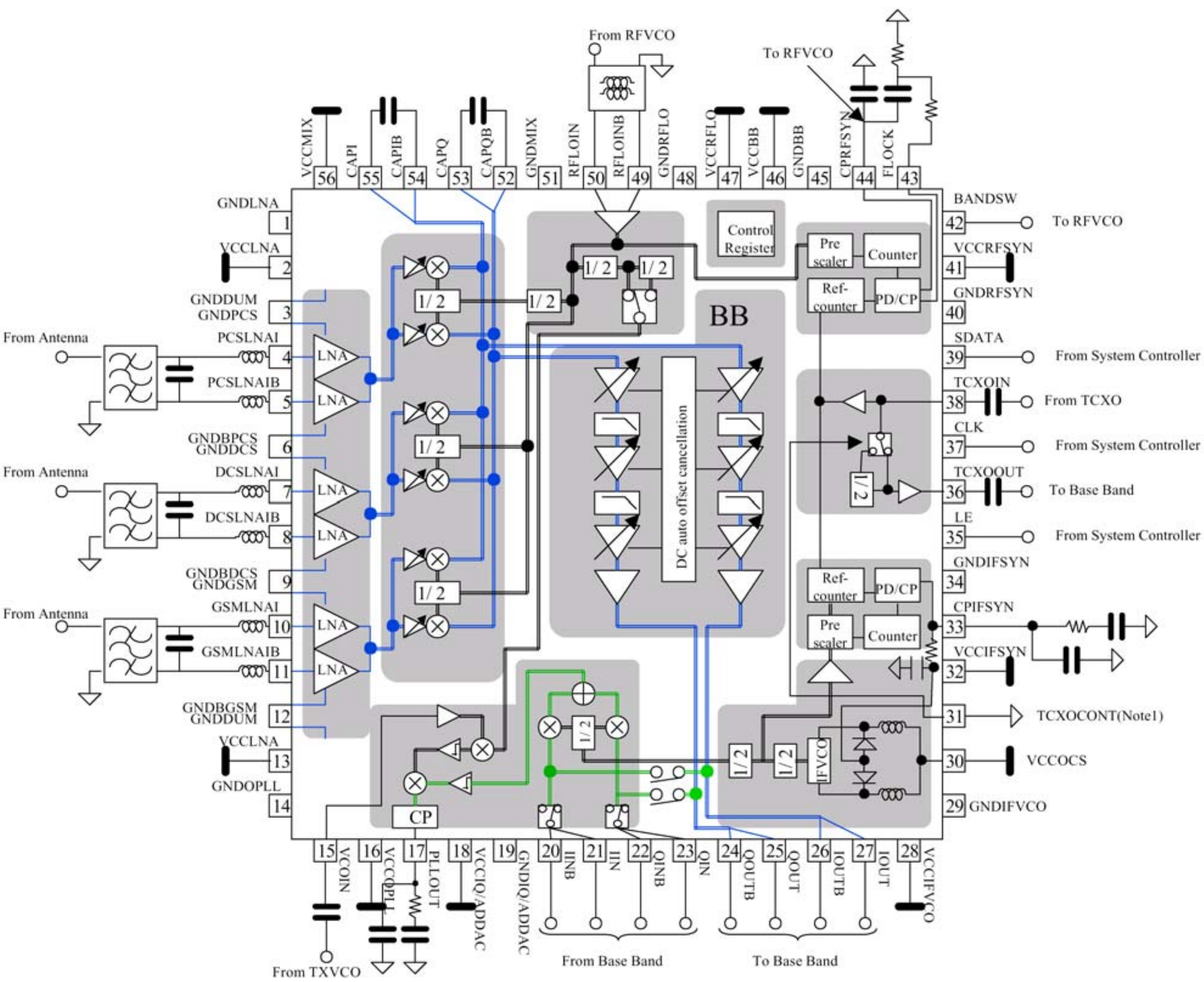


### 4.4.2 IC Overview

IC Overview

BRIGHT IV

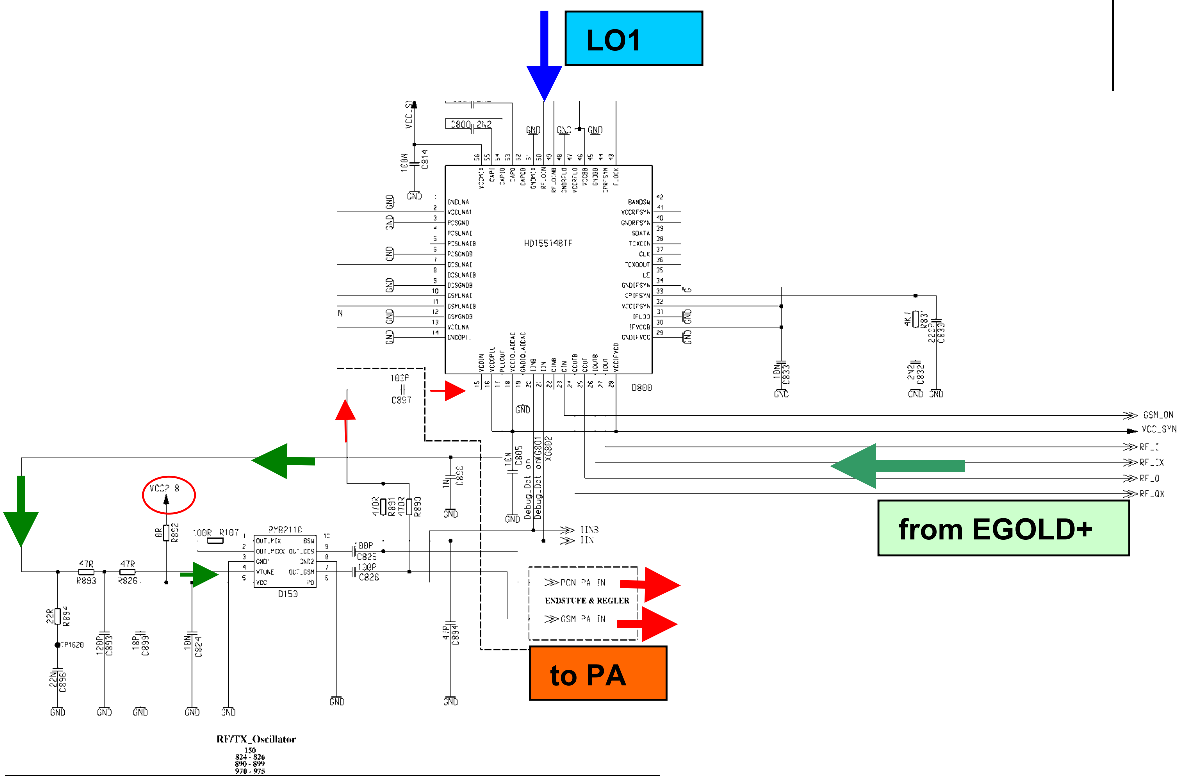


# 4.5 Transmitter

## 4.5.1 Transmitter: Modulator and Up-conversion Loop

The modulation is based on the principle of the “up-conversion modulation phase locked loop” and is accomplished via the BRIGHT IC(D800). An internal TX IF-LO provides the quadratic modulator with the TX IF frequency of 80/82 MHz by generating 640/656MHz divided by 8. This so generated IF GMSK RF signal is compared in a phase detector with the down mixed GMSK RF output from the TX-VCO (Z150). To get the comparison signal, PCN_PA_IN (for GSM1800), and GSM_PA_IN (for EGSM900) appearing at Pin 9/7 of the (D150) are mixed with the LO1 signal (divided by 2 for GSM1800 and 4 for EGSM900). The output (PLLOUT) signal of the phase detector passes a discrete loop filter realised by capacitors and resistors to set the TXVCO to required frequency. The large loop band width (~1,5MHz) guarantees that the regulating process is considerably quicker than the changes in the modulation signal.

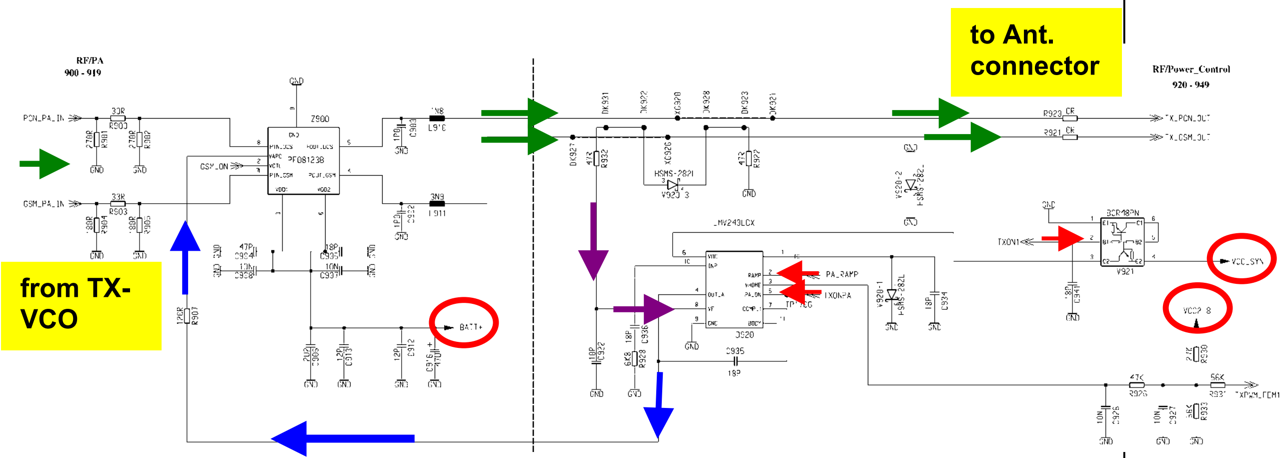
The required voltage VCC_SYN and VCC2_8 is provided by the ASIC D361



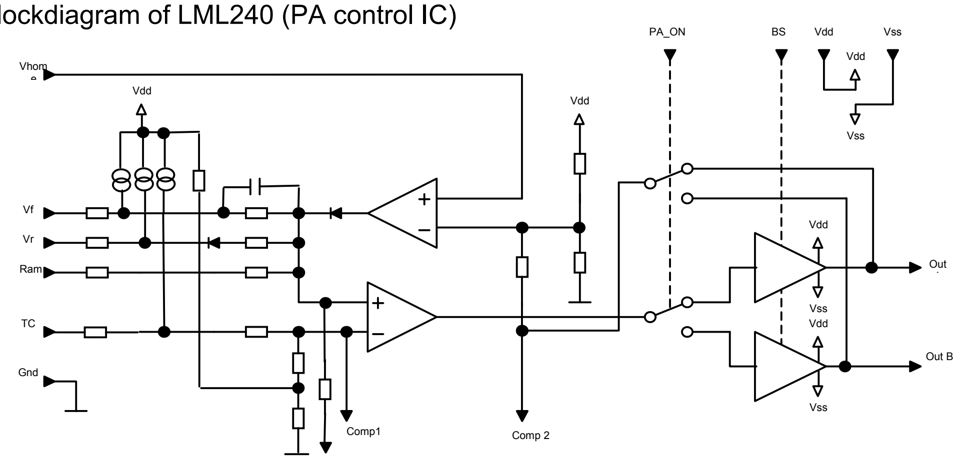
### 4.5.2 Transmitter: Power Amplifier

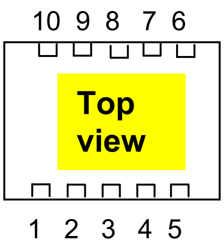
The output signals (PCN_PA_IN , and GSM_PA_IN) from the TX-VCO are led to the power amplifier (Z900) passing a matching circuit. The PA is a “two in one” PA (EGSM900/GSM1800) and is connected directly to Batt+. The band selection switching is done via GSM_ON from the Bright IC. After amplification, a part of the output signals (TX_PCN_OUT and TX_GSM_OUT) is decoupled via a directional coupler. The other part runs through the antenna switch (Z880) inside the FEM and the antenna connector (X870) to the Antenna. The decoupled part is equalised by the detector diode (V920) and used from the RF-Power regulator IC (D920) to get a PA control voltage, by comparing this voltage with the PA_RAMP signal provided from the EGOLD+ (analogue interface J2). The (N920) is activated through the signal TXON1. TXONPA enables with a “high” signal the output “a” (pin 4).

The required voltage BATT+ is provided by the battery.
The required voltage VCC2_8 is provided by the ASIC D361.




Blockdiagram of LML240 (PA control IC)



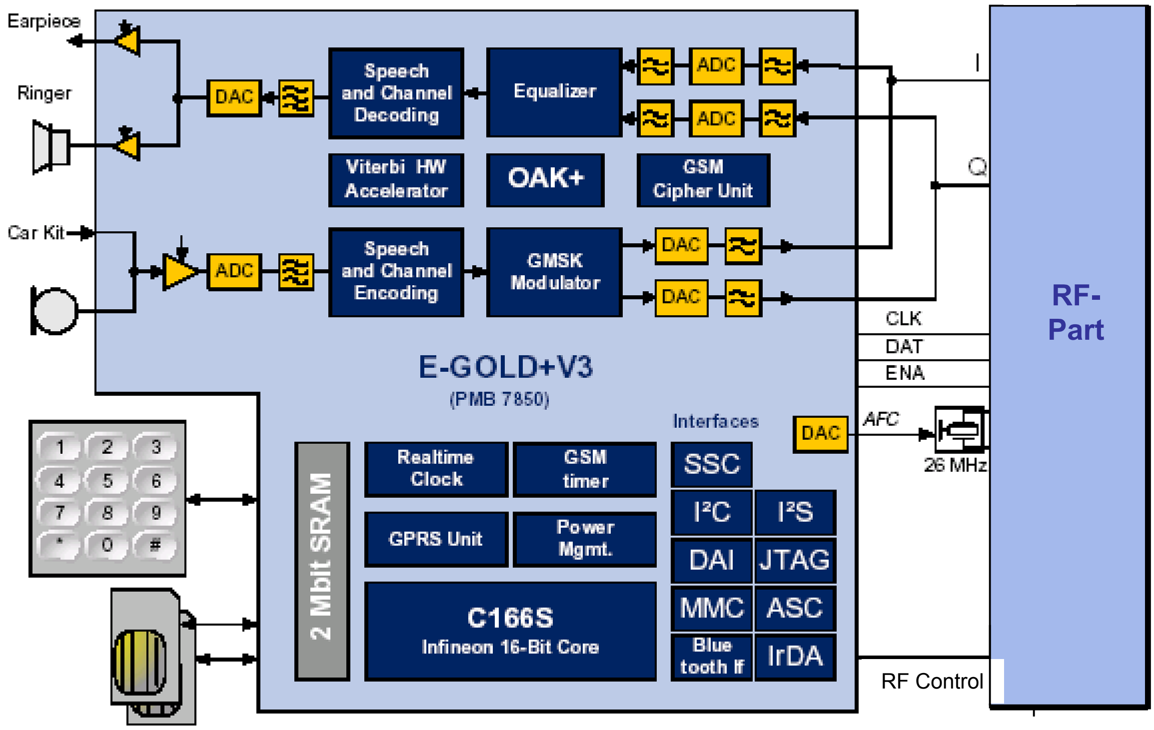



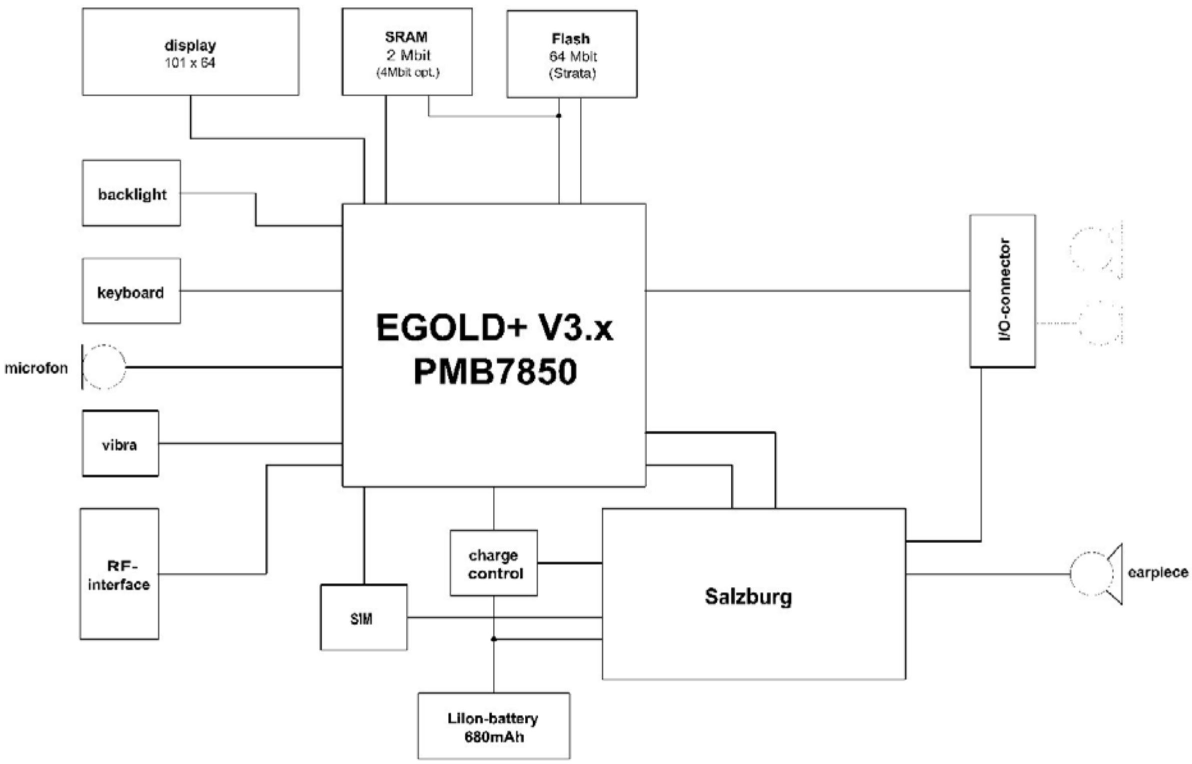
# 5 Logic / Control

## 5.1 Overview of Hardware Structure

### 5.1.1 Logic Block Diagram



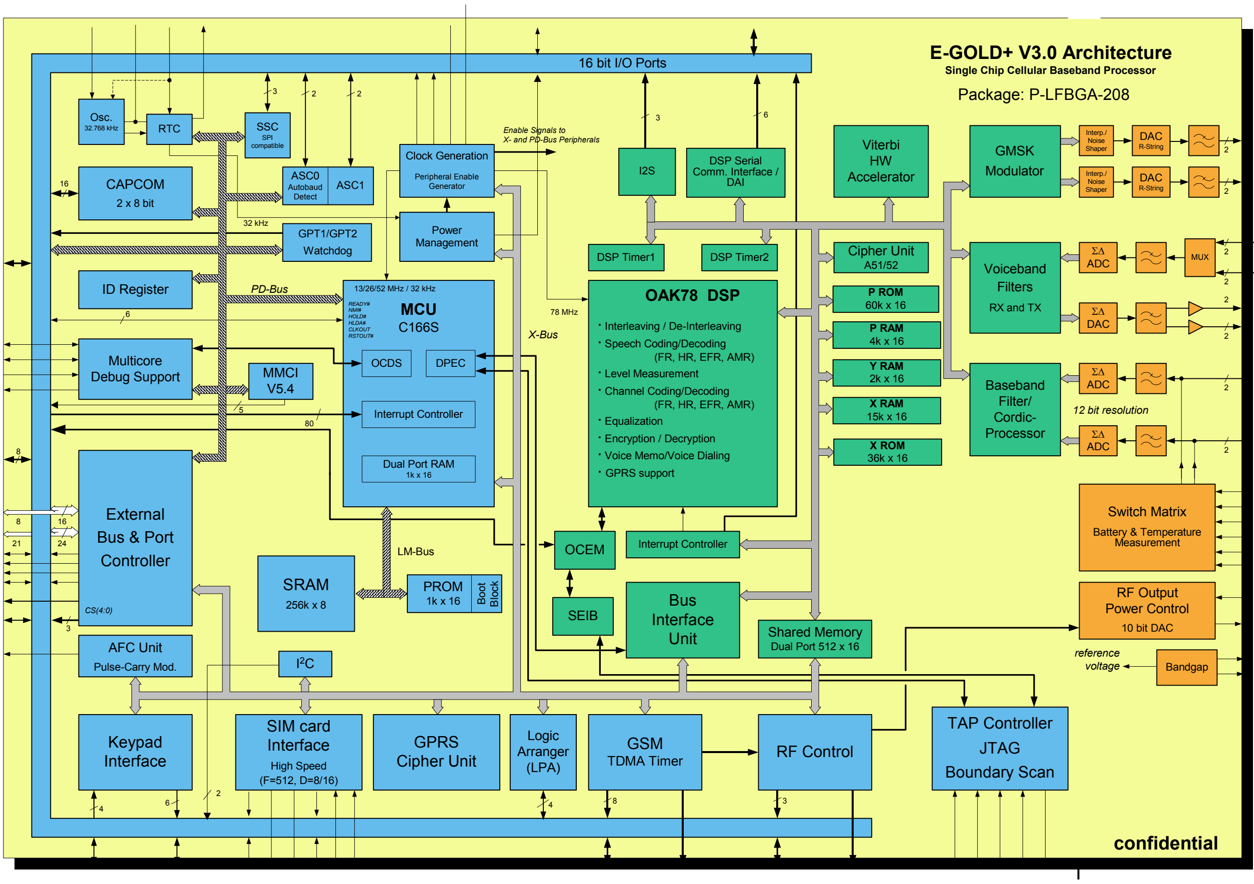

### 5.1.2 Block Diagram A55/C55 Control Part



### 5.1.3 EGOLD+

Block Diagram EGOLD+ V3.1




The EGOLD+ contains a 16-bit micro-controller (µC part), a GSM analog Interface (EGAIM), a DSP computing core (DSP part) and an interface for application-specific switch-functions.

<u>The µC part consists of the following:</u>

- Micro-controller
- System interfaces for internal and external peripheries
- On-chip peripheries and memory

<u>The Controller Firmware carries out the following functions:</u>

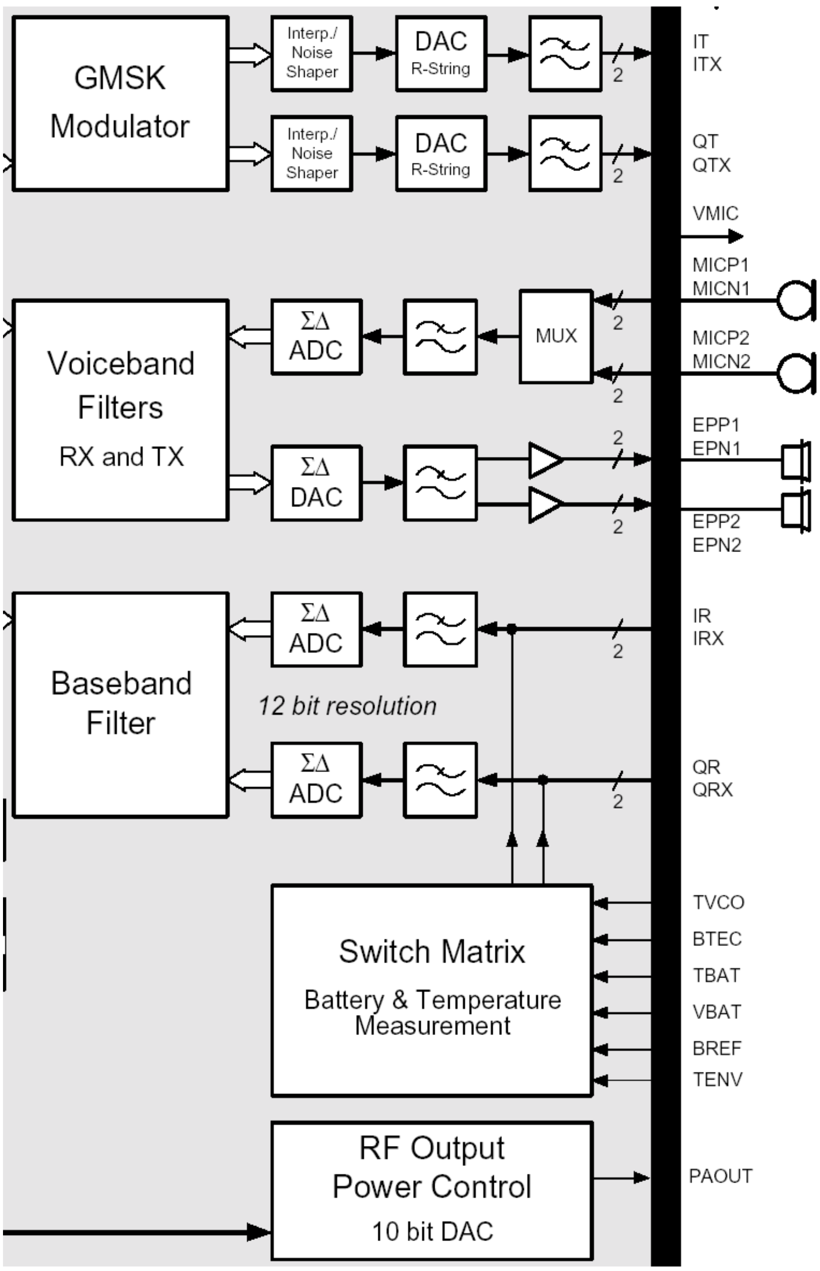
- Control of the Man Machine Interface (keypad, LCD, sensing element, control of the illumination,...)
- GSM Layer 1,2,3 /GPRS
- Control of radio part (synthesizer, AGC, AFC, Transmitter, Receiver...),
- Control of base band processing (EGAIM)
- Central operating system functions (general functions, chip select logic, HW driver, control of mobile phones and accessories...).

The EGAIM part contains the interface between the digital and the analogue signal processing:

- 2 Sigma Delta A/D converters for RX signal, and for the necessary signals for the charge control and temperature measurement. For this, the converter inputs are switched over to the various signals via the multiplexer.
- 2 D/A converters for the GMSK-modulated TX signal,
- 1 D/A converter for the Power Ramping Signal,
- 1 Sigma Delta A/D and D/A converter for the linguistic signal.

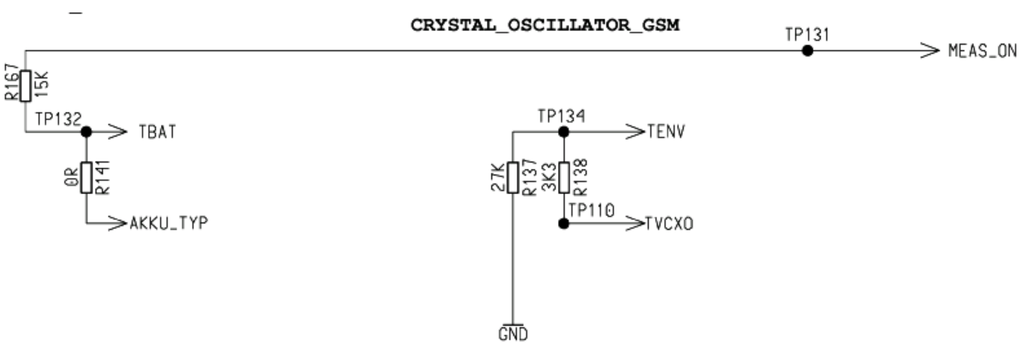
Blockdiagram EGAIM inside the EGOLD



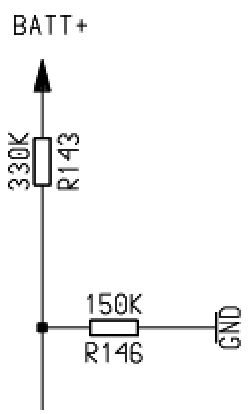
**Measurement of Battery and Ambient Temperature**

The battery temperature is measured via the voltage divider R1387, R138 by the EGOLD+ (Analog Interface P2). For this, the integrated ΣΔ converter of the RX-I base band branch is used. This ΣΔ converter compares the voltage of TBAT and TENV internally. Through an analogue multiplexer, either the RX-I base band signal, or the TBAT signal and the TENV signal is switched to the input of the converter. The signal MEAS_ON from the EGOLD+(GSM TDMA-TIMER H15) activates the battery voltage measurement The ambient temperature TENV is measured directly at of the EGOLD+ (Analog Interface P3).




**Measurement of the Battery Voltage**

The measurement of the battery voltage is done in the Q-branch of the EGOLD+, for this BATT+ is connected via a voltage divider R143, R146 to the EGOLD+(Analog Interface P1). An analogue multiplexer does the switching between the baseband signal processing and the voltage measurement.



### A/D conversion of MIC-Path signals incl. coding

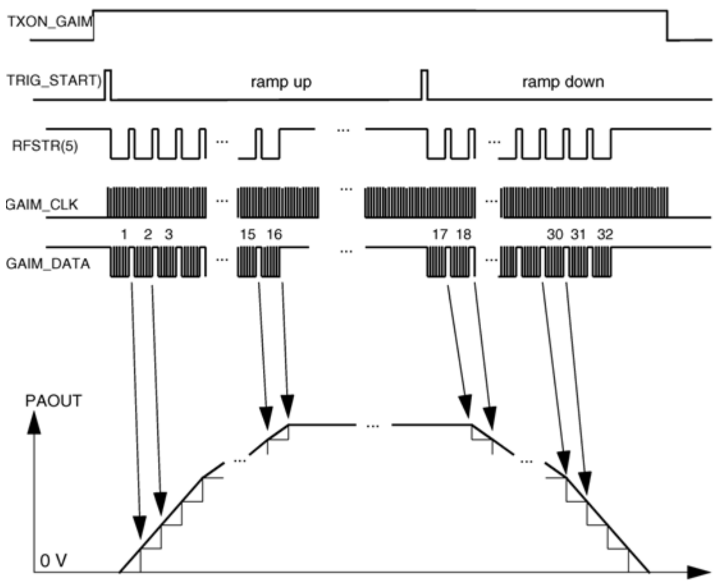
The Microphone signals (MICN2, MIP2, MICP1, MICN1) arrive at the voiceband part of the EGOLG+. For further operations the signals will be converted into digital information, filtered, coded and finally formed into the GMSK-Signal by the internal GMSK-Modulator. This so generated signals (RF_I, RF_IX, RF_Q, RF_QX) are given to the Bright IC in the transmitter path.

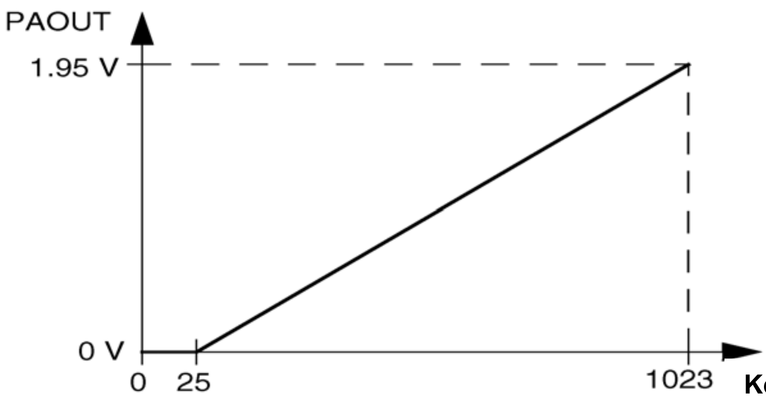
### D/A conversion of EP-Path signals incl. decoding

Arriving at the baseband-Part the demodulated signals (RF_I, RF_IX, RF_Q, RF_QX) will be filtered and A/D converted. In the voiceband part after decoding (with help of the µC part) and filtering the signals will be D/A converted amplified and given as (EPP1_FIL, EPN1_FIL) to the Power Supply ASIC.

### Generation of the PA Control Signal (PA_RAMP)

The RF output power amplifier needs an analogue ramp up/down control voltage. For this the system interface on EGOLD+ generates 10 bit digital values which have to be transferred serially to the power ramping path. After loading into an 10 bit latch the control value will be converted into the corresponding analogue voltage with a maximum of ~2V



The DSP part contains:

- DSP signal processor
- Separate program/data memory
- a hardware block for processing the RX signal,
- a hardware block for “ciphers“,
- a hardware block for processing the linguistic signal,
- a hardware block for the “GMSK modulator“,
- De-/ interleaving memory,
- Communication memory
- a PLL for processing and reproducing the VCXO pulse signal.

In the DSP Firmware are implemented the following functions:

- scanning of channels, i.e., measurement of the field strengths of neighbouring base stations
- detection and evaluation of Frequency Correction Bursts
- equalisation of Normal Bursts and Synchronisation Bursts
- channel encoding and soft-decision decoding for fullrate, enhanced-fullrate and adaptive multirate speech, fullrate and halfrate data and control channels.
- channel encoding for GPRS coding
- fullrate, enhanced fullrate and adaptive multirate speech encoding and decoding
- mandatory sub-functions like
  – discontinuous transmission, DTX
  – voice activity detection
  – background noise calculation
- generation of tone and side tone
- hands-free functions
- support for voice memo
- support for voice dialling
- loop-back to GSM functions
- GSM Transparent Data Services and Transparent Fax
- calculation of the Frame Check Sequence for a RLP frame used for GSM NonTransparent Data Services
- support of the GSM ciphering algorithm

Real Time Clock (integrated in the EGOLD+):
The real time clock is powered via a separate voltage regulator inside the Power Supply ASIC. Via a capacitor, data are kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with which it is possible to switch the phone on and off.

### 5.1.4 SRAM

Memory for volatile data
Memory Size: 4 Mbit
Data Bus: 16Bit

### 5.1.5 FLASH

Memory Size: 64Mbit (8 Mbyte)
Data Bus: 16 Bit

### 5.1.6 SIM

SIM cards with supply voltages of 1.8V and 3V are supported.

### 5.1.7 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts.

# 6 Power Supply

## 6.1 Power Supply ASIC

The power supply ASIC will contain the following functions:

• Powerdown-Mode
• Sleep Mode
• Trickle Charge Mode
• Power on Reset
• Digital state machine to control switch on and supervise the µC with a watchdog
• Voltage regulator
• Low power voltage regulator
• Additional output ports
• Voltage supervision
• Temperature supervision with external and internal sensor
• Battery charge control
• I2C interface
• Audio multiplexer
• Audio amplifier stereo/mono
• 16 bit Sigma/Delta DAC with Clock recovery and I2S
• Bandgap reference*

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**INFO:**

*** Bandgap reference**

The p-n junction of a semiconductor has a bandgap-voltage. This bandgap-voltage is almost independent of changes in the supply voltage and has a very low temperature gradient. The bandgap-voltage is used as reference for the voltage regulators.

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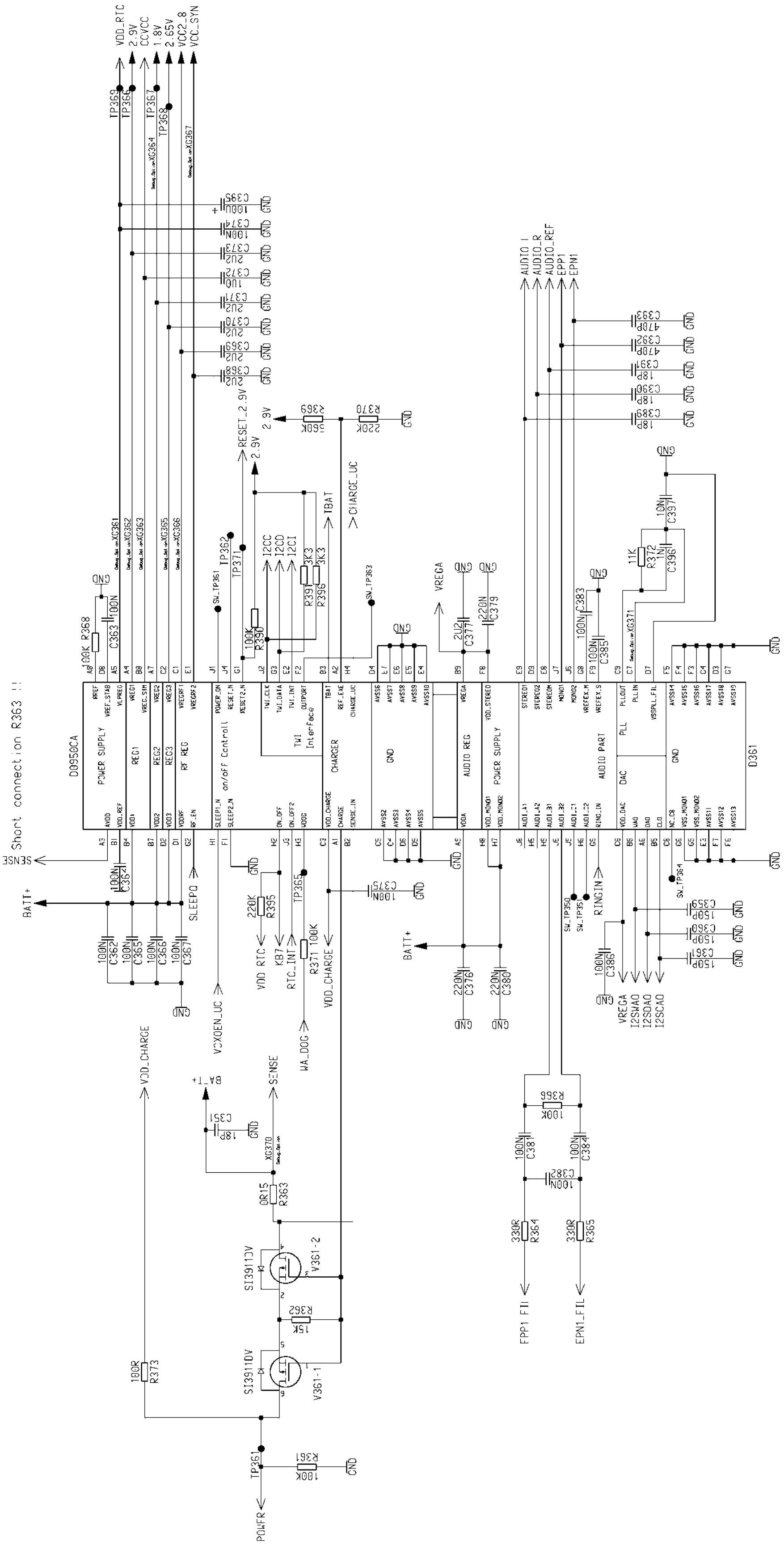
### 6.1.1 Power Supply Diagram



### 6.1.2 Power Supply Operating modes:

The ASIC can be used in different operating modes:

| Mode | Pin Requirements | Description |
|---|---|---|
| Power down mode with minimum activity | ON/OFF<br>ON/OFF2<br>VDD_CHARGE | In power down mode the current consumption of the ASIC is very low. The inputs for switch on conditions (ON/OFF-PinH2, ON/OFF2-PinJ3 ,VDD_CHARGE-PinC3), the LPREG, Bandgap reference and the POR cells are active. All other blocks are switched off, so the battery is not discharged. This state is called "phone off. |
| Start Up Mode | ON_OFF<br>ON_OFF2 | Start Up Mode can be initiated by ON_OFF(PinH2) or ON_OFF2(PinC3). In this mode a sequential start-up of references, oscillator, voltage supervision and regulators is controlled by digital part. In failure case (under voltage, over voltage or time out of the µC reaction)., the ASIC is shut down. |
| Full operating mode | VDD_CHARGE<br>CHARGE_UC | All blocks are active. Trickle charge is switched off. The blocks fast charge and charge monitor can be active only in this mode. These modes will be activated with VDD_CHARGE(PinC3) or CHARGE_UC(PinH4). The name of this mode is "phone on" or "active mode". The border between the startup phase and the active mode is the rising edge of the RESET2_N (PinG1) signal. This will allow the µC(EGOLD+) to start working. |
| Active Mode (submode of Full operating mode) | | In this mode, the µC(EGOLD+) controls the charging block and most of the failure cases. The ASIC can be controlled by the TWI interface (I2CC-PinJ2, I2CD-PinG3, I2CI-PinE2), interrupts can be sent by the ASIC. Further, the temperature and the voltages are supervised (in case of failure, the uC will be informed). In case of watchdog failure, over voltage or power on reset, the ASIC will be switched off immediately. The mono and stereo audio block can be switched on in active mode. |
| Sleep Mode with special low current operating mode for the LDOs (submode of Full operating mode) | SLEEP1_N<br>TC_ON<br>CHARGE_uC | A low level at the signal VCOEN_UC (PinH1) will switch the phone from the mode "PHONE ON" to sleep mode. This mode can be activated out of the active mode. In sleep mode trickle charge, fast charge, supply over voltage detection, supply under voltage detection, audio function are switched off. LDO under voltage detection, clock and all reference voltages are active. LDOs are working in low current mode. The possibility to supply the ASIC from VDD_CHARGE (PinC3) with the internal LDO is switched off. Only the battery can be used for supply. This mode is called "phone stand-by". |

| Mode | Pin Requirements | Description |
|---|---|---|
| Trickle charge mode to be able to support charging of the battery | VDD_CHARGE EXT_PWR | In case of a rising edge at VDD_CHARGE (PinC3) the ASIC goes from power down to interim mode. In this mode, the oscillator and the reference are started. The fuses are read in. If the voltage is high enough (after a delay time of 1 ms to filter a ringing), the internal signal EXT_PWR is going to H and the power up continues. The ASIC shuts off if the voltage is below threshold. In Trickle Charge Mode, first the charge unit starts and charges the battery in case of under voltage. After reaching this threshold voltage or if the battery has enough voltage from the beginning, a start up similar to the regular startup mode is initiated. In case of voltage drop under battery threshold, the first trickle charging can be started again until the Active Mode is entered. In this case, the internal VDDREF regulator, the reference generator and oscillator are started and the ASIC is supplied by VDDREF. If any failure is detected, the ASIC is switched off. |

### 6.1.3 Power Supply Functions:

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Switching on the mobile phone | ON_OFF, ON_OFF2, VDD_CHARGE | There are 3 different possibilities to switch on the phone by external pins:<br>- VDD_CHARGE (PinC3) with rising edge after POR or high level at end of POR signal<br>- ON/OFF (PinH2) with falling edge<br>- ON/OFF2 (PinJ3) with rising edge<br>In order to guarantee a defined start-up behavior of the external components, a sequential power up is used and the correct start up of these blocks is supervised. In active mode, a continuous signal at watchdog is needed to keep the system running. If the signals fails, the ASIC will switch to power down mode. It must be guaranteed that each start-up condition does not interfere and block the other possible startup signals. In case of failure during start-up, the device will go back to power down mode. To guarantee that VDDCHARGE (PinC3) is always sensed we must be able to detect whether the VDDCHARGE (PinC3) will have a rising edge during POR (this can happen in case of an empty battery). Therefore this signal is sensed as level sensitive at the end of POR and edge sensitive after POR signal. |

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Watchdog monitoring | WDOG | As soon as the first WDOG (PinH3) pin rising is detected during the TE4 timer, the device start the watchdog monitoring procedure. Standard switch off of the phone is the watchdog. The first edge of watchdog is rising. If a falling edge is detected as the first transient the device will go to power down mode again and the whole phone is switched off. Rising and falling edges must be detected alternated. With any edge on WDOG (PinH3) pin a counter will be loaded. The next - compared to the previous edge - inverted edge must occur between end of T1, and end of T2. If the signal occurs before end of T1 or is not detected until end of T2, the device will go to power down mode immediately after the violation of the watchdog criteria occurs.<br>T1 min. 0,327s/ typ. 0,360s/ max. 0,400s<br>T2 min. 2,600s/ typ. 2,860s/ max. 3,178s |
| Power-On-Reset (POR) | RESET_N<br>RESET2_N | To guarantee a correct start-up of the ASIC, a power on reset is needed at first power supply ramping. Therefore a static/dynamic power on reset circuit is added, which creates a reset each time the power supply is connected. After POR the ASIC starts up the reference and the oscillator, read in the fuse content and goes back to power down mode. If the power supply will drop under the POR threshold a synchronous reset is done and the ASIC will go to power down mode independently of the previous operating mode. |
| Voltage Supply Logics | REG1<br>(2.9V) | The linear controller is designed for 2.9V(±2%) and a maximum load current of 140 mA.<br>Voltage and current for the external Logic is supplied from the internal 2.9V logic regulator. The operating voltage VREG1 is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference |
| Voltage Supply Logics | REG2<br>(1,92V) | The linear controller is designed for 1.82V(±3%) and a maximum load current of 300 mA.<br>The REG2 supplies the Baseband Processor. For a high power application, the power has to be dissipated outside of the chip. This is done with a series diode at the input of REG2, which will force the regulator to a lower input voltage and therefore lower power dissipation. |

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Voltage Supply Logics | REG3 (2.65V) | The linear controller is designed for 2.65V(±3%) and a maximum load current of 220 mA.<br>It will consist basically of an internal operation amplifier, an integrated p-channel output transistor as well as a capacitor (C = 2.2µF) for stabilizing the voltage. The required reference voltage for the regulating circuit will be generated internally via a bandgap. The negative feedback of the regulating circuit shall be done via chip-internal resistances. |
| Voltage Supply RF | VREGRF1, RF_EN, RESET_N | The linear controller is designed for 2.85V(min. 2.79V, max. 2.91V) and a maximum load current of 120 mA.<br>Voltage and current for RF-VCO and Transceiver is supplied from the internal 2.85V LDO. The operating voltage RF12LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed.<br>RF1LDO is controlled by RF_EN. If it is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF1LDO can only be enabled by TWI bit. In external mode, RF1LDO can only be enabled by RF_EN.<br>RF1LDO is released with rising edge of RESET_N signal. |
| Voltage Supply RF | VREGRF2, SLEEP1_N, SLEEP2_N, POWER_ON | The linear controller is designed for 2.85V(min. 2.79V, max. 2.91V) and a maximum load current of 180 mA.<br>Voltage and current for RF-VCO and Transceiver is supplied from the internal 2.85V LDO. The operating voltage RF2LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed.<br>RF2LDO is controlled by VCXO_EN (PinH1). If it is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF2LDO can only be enabled by TWI bit. In external mode, RF2LDO can only be enabled by VCXO_EN (PinH1).<br>RF2LDO is released with rising edge of POWER_ON signal. |

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Voltage Supply Audio | VREGA | The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 190 mA.<br>BATT+ (PinA9) is used for the whole stereo analog supply. The DAC digital VDDDAC (PinC6), Low Noise Bandgap, Mono- and Stereoamplifier supplies are connected to VREGA (PinB9). The AUDIO performances are guaranteed only, if the VREGA supplies all the stereo path.<br>VREGA is controlled with TWI registers directly by the µC. |
| Voltage Supply RTC | VLPREG | The linear controller is designed for 2.00V(min. 1.9V, max. 2.1V) and a maximum load current of 1 mA.<br>The output voltage can be adjusted to four different values with TWI register by the µC. The selectable values are 2.00(default), 1.82, 1.92 and 2.07V. LP-LDO is always working and will switch of only with POR signal. |
| Voltage Supply SIM | VREGSIM | The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 60 mA. The output voltage can be adjusted to a different value with TWI register by the µC to 1.8V(min. 1.76V, max. 1.84V).<br>This regulator can be activated by TWI register , but only in active mode. If the regulator is in power down, the output is pulled down by a transistor to avoid electrostatic charging of VREGSIM (PinB8) |
| Charge Support | CHARGE_UC, CHARGE, VDDCHARGE, AVDD, SENSE_IN, TBAT | A charge support will be integrated for controlling the battery charge function. It consists basically of a temperature sensor, an external charge FET, an integrated High-side driver for the external FET with an external resistor between the source and the gate of the charge FET.<br>In the case of a rising edge at the CHARGE_UC(PinH4) the power source will be switched on. In this way the charge FET becomes conducting, provided that the integrated temperature comparator does not give the signal for extreme temperature and that no over voltage is present at the VDD. In the case of falling slope at the CHARGE_UC(PinH4), the current source is switched off and the pull-up resistor will make sure that the charge FET is blocked after a definite time.<br>Temperature switchoff becomes effective at approx. T>60°C. |
| Voltage supervision | | The levels of regulator REG1 and REG2 and also the supply voltage BATT+ are supervised with comparators. |

| Functions | Pin Requirements | Sequence |
| --- | --- | --- |
| Supervision of REG1 and REG2 | REG1<br>REG2 | In active mode the regulators are supervised permanently. If the voltage is under the threshold, the pin RESET_N2 (PinG1) stay Low and the ASIC goes back to the power down mode. If the voltage is longer than Tmin under threshold voltage, the RESET_N2 (PinG1) is going to Low (Missing Watchdog signal -> phone switched off). The level of regulator REG1 and REG2 will be supervised permanently. If the voltage doesn't reach the threshold value at switch on, the RESET_N2 (PinG1) will stay low and the ASIC will go back to power down mode. The voltages are sensed continuously and digitally filtered with a time constant Tmin. If the regulator voltage is under threshold longer than Tmin, the RESET_N2 (PinG1) signal change to low and the µC will go to RESET condition (Missing Watchdog signal -> phone switched off). |
| Powersupply supervision | VDD | If the battery voltage BATT+ exceeds VDD high, everything is switched off immediately within 1µs. Only the pull-up circuitry for the external charge PMOS are active and will discharge the gate of the external PMOS |
| VDDA supervision | VDDA | To provide a short circuit protection at output of VDDA (PinA9) and output of stereo buffer a voltage supervision is implemented. If the VDDA output is less then this threshold, the VDDA will be switched off for 128ms. After this time the VDDA will be started again. The VDDA supervision starts 60ms after startup of VDDA. |
| Battery temperature supervision | | Charging is stopped, when over temperature occurs. Within 128ms, 3 values are measured. When these 3 values are identical status can be changed. The supervision is active in fast charge or trickle charge mode. Voltage on pin TBAT (PinB3) becomes smaller when temperature increases. If Vbat < (Vref_exe - Vhyst) charging is disabled. Only when Vtbatt > Vref_exe charging is enabled again. |
| Device temperature supervision | | To protect the ASIC, the temperature is supervised. The temperature is polled every 128ms and is filtered as in battery temperature supervision. If over temperature is detected, a bit in the STATUS register is set and an interrupt is generated. Monitoring is started only in active mode. |
| Analog switch Outport | | The level can be defined by the bit out_port_high of the TWI register. The high level can be derived of VREG2 or VREG3. Additional a pull down transistor is connected to this node. |
| TWI Interface | TWI_CLK,<br>TWI_DATA,<br>TWI_INT | The TWI interface (I2CC-PinJ2, I2CD-PinG3, I2CI-PinE2) is an I2C compatible 2-wire interface with an additional interrupt pin to inform the µC about special conditions.<br>The interface can handle clock rates up to 400 kHz. |

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Audio mode functions | | Four audio amplifiers are integrated to support these modes:<br>1. Supply the speaker in the phone with audio signals including the possibility of handsfree switch on and off. This is the AUDIO MONO MODE.<br>2. Supply the speaker in the phone with ringing signal (RINGER MODE)<br>3. Transfer a key click, generated in digital part to the speaker. (KEY-CLICK FUNCTION)<br>4. Supply of stereo head set with stereo signal with short circuit protection. This is called the AUDIO STEREO MODE. These different modes with gain and multiplexing can be controlled via TWI. Also the output can be switched to TRI-STATE via TWI interface. |
| Audio Mono Mode | VREGA<br>MONO1<br>MONO2<br>VREFEX_M | This mode is the main function of the amplifier. The two amplifiers are used as differential mono amplifier to drive the speaker in the phone as external load. This differential approach allows delivering an optimum of power to the speaker also in low voltage mode. Both amplifier paths are inverting amplifiers with external AC coupling at the input to compensate offset failures. The gain can be adjusted with the TWI interface. The output stage of the amplifiers must be able to drive a low impedance load as an external speaker for the handsfree application.<br>General parameters: Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB. The signals for the amplifier are connected via an audio multiplexer with 3 pairs of input signals. |
| Ringer function | RINGIN | In ringer mode the ringing signal is transferred via the amplifier to the speaker to eliminate the additional buzzer. The speaker is controlled with a rectangular signal RINGIN (PinG9). Input signal is digital signal with variable frequency. Amplitude is adjusted by TWI register.<br>For start-up a smaller time constant must be used to allow a fast switch on behavior. Ringing function can be started at any time. If the audio is off, the start-up is done with RINGER time constant. If audio is starting with AUDIO start-up, the time constant is switched to RINGER mode, too. If the audio amplifier is already up and running, the RINGIN (PinG9) is connected to the amplifier and audio signal is muted due to open multiplexer. |

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Key click function | | Pushing a key of the phone can be combined with a key click. This function is also realized with the audio amplifier in pulsed mode. The ASIC creates a digital PWM signal. Frequency of the PWM signal is 3.5 kHz.<br>The start-up is similar to the ringer function. If the audio is off, the start-up is done with KEYCLICK time constant. If audio is starting with AUDIO start-up, the time constant is switched to KEYCLICK mode, too. If the audio amplifier is already up and running, the KEYCLICK is connected to the amplifier and audio signal is muted due to open multiplexer. |
| Audio Multiplex Matrix | AUDIOA1<br>AUDIOA2<br>AUDIOB1<br>AUDIOB2<br>AUDIOC1<br>AUDIOC2 | Each of the three input sources should be switched to Mono and Stereo outputs. Furthermore a conversion can be done.<br>Following sources:<br>- Mono differential<br>- Mono Single Ended (both channels parallel)<br>- Stereo<br>The DAC can be switched off for using the analog external inputs. This principle will allow to do each combination and have different modes for stereo and mono in parallel. |
| I2S Interface | CLO,<br>WAO,<br>DAO | The I2S Interface is a three-wire connection that handles two time multiplexed data channels. The three lines are the clock (CLO), the serial data line (DAO) and the word select line (WAO). The master I2S also generates the appropriate clock frequency for CLO set to 32 times the sampling rate (FS) |
| Audio DAC | VDDDAC | For digital to analog conversion a 16-bit sigma delta converter is used. Digital input signal is delivered with an I2S interface. The I2S interface should be 16-bit format. To be able to work with all possible operating modes, the sampling frequency can vary from 8kHz to 48kHz. The performance of the audio output signal must be guaranteed over the full range the human ear is able to hear. This means for FS=8kHz the noise at frequencies higher than FS/2 must be suppressed. This is done by DSP and a single ended 2$^{nd}$ order Low Pass filter. The clock for the I2S will be varied accordingly to the sampling frequency. Therefore a clock recovery based on CLO signal of the I2S can be implemented. This clock recovery must smooth any jitter of this clock to reduce the noise of the DAC. |
| PLL | VDDPLL<br>PLLOUT | The PLL will have three frequency modes to produce a 32xCLO clock for the DSP and the DAC. The loop filter is realized with an external RC circuit. This PLL also contains a lock detector circuit. |

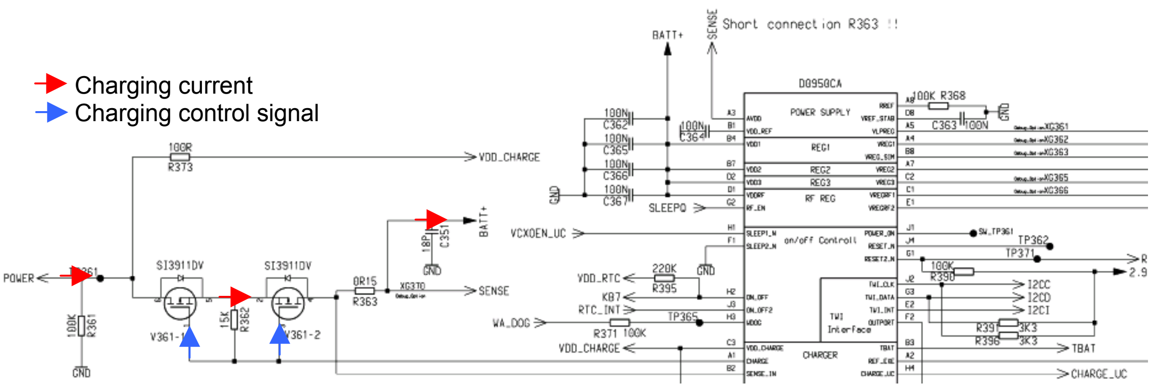
  

| Functions | Pin Requirements | Sequence |
|---|---|---|
| Audio Stereo Mode | VDDSTEREO<br>STEREO1<br>STEREO2<br>STEREOM | For stereo mode 2 single ended buffers are used. These buffers will be supplied by the additional regulator with 2.9 Volt to be more stable against the GSM ripple on the battery voltage. Also reference voltage for the buffers is generated by a high precision, low noise bandgap reference for better performance. An external capacitor is needed to filter this reference additionally. The gain steps for the programmable gain amplifier is identical with the mono amplifier. No keyclick and ringer needed for the stereo part. Gain can be controlled with the TWI. The connected speaker has an impedance of typical 16 Ohm. To guarantee an ANTI-POP noise a digital startup is implemented. This will allow a soft start of the VMID and creates a “clean” audio band during the startup. For eliminating external coupling capacitors for the speaker, an additional amplifier creates virtual ground (for both speakers). Accordingly to this, the max current of the virtual ground has to be the double of the normal output amplifier. Due to the power amplifier offset a DC current appear in the headset. Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB |

## 6.2 Battery

As a standard battery a LiIon battery with a nominal capacity of 3,7 Volt/700mAh is used.

## 6.3 Charging Concept



#### 6.3.1.1 Charging Concept

**General**

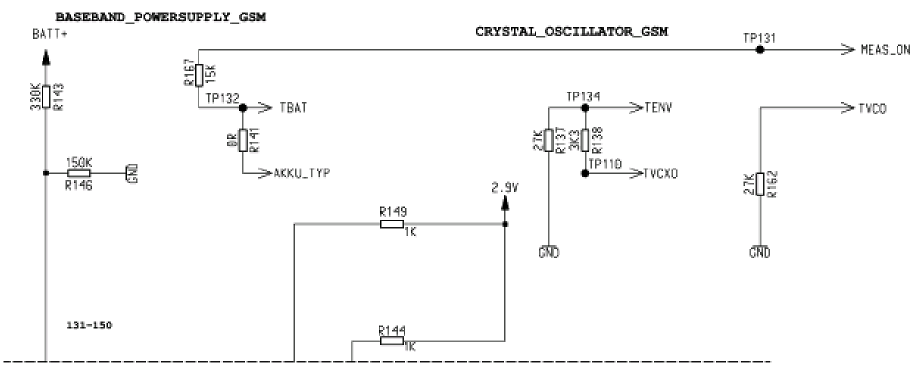
The battery is charged in the unit itself. The hardware and software is designed for LiIon with 4.2V technology.
Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging takes place in the background (the customer can see this via the “Charge” symbol in the display). During normal use the phone is being charged (restrictions: see below).
Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The EGOLD+ takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the POWER SUPPLY ASIC hardware can override/interrupt the charging in the case of over voltage of the battery (only for Manganese Chemistry Battery types e.g. NEC).
With the new slim Lumberg IO connector we lose the charger recognition via SB line. Now we measure the charge current inside the POWER SUPPLY ASIC with a current monitor.
The charging software is able to charge the battery with an input current within the range of 350-600mA. If the Charge-Fet is switched off, then no charging current will flow into the battery (exception is trickle charging, see below).
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. The NTC for the ambient temperature will be on the PCB (13 MHz part).

**Measurement of Battery, Battery Type and Ambient Temperature**

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the EGOLD. For this, the integrated ΣΔ converter in the EGOLD of the RX-I base band branch will be used. Via an analogue multiplexer, either the RX-I base band signal, the battery code voltage or the ambient temperature voltage can be switched over to the input of the converter. The 1-Bit data stream of the converter will be subjected to a data reduction via the DSP circuit so that the measured voltage (for battery and ambient temperature) will be available at the end as a 10-bit data word.

**Measurement of the Battery Voltage**

Analogue to the I-branch either the RX-Q base band signal or the battery voltage can be measured in the Q-branch. Processing in the DSP circuit will be done analogue to the I-branch. The EGOLD will be specified internally at voltage measurement input BATT+ for an input voltage of 3V...4.5V.



### Timing of the Battery Voltage Measurement

Unless the battery is charging, the measurement is made in the TX time slot. During charging it will be done after the TX time slot. At the same time, either the battery temperature (in the I-branch) and the battery voltage (in the Q-branch) or the ambient temperature in the I-branch can be measured (the possibility of measurement in the Q-branch, the analogue evaluation of the battery coding, is used for HW-Coding). Other combinations are not possible. For the time of the measurement the multiplexer in the EGAIM must be programmed to the corresponding measurement.

### Recognition of the Battery Type

The battery code is a resistor with a resistance depending on the manufacturer.

### Charging Characteristic of Lithium-Ion Cells

LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is approx. 600mA, minimum about 100mA. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be started ranges from 5...40°C, and the temperature at which charging takes place is from 0...45°C. Outside this range no charging takes place, the battery only supplies current.

### Trickle Charging

The POWER SUPPLY ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the POWER SUPPLY ASIC. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.75V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the POWER SUPPLY ASIC will switch on the phone automatically and normal charging will be initiated by software (note the restrictions on this item as stated below).

### Normal Charging

For battery voltages above 3.2 Volt and normal ambient temperature between 5 and 40°C the battery can be charged with a charge current up to 1C*. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the POWER SUPPLY ASIC. The level of charge current is limited/controlled by the accessory or charger.

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**INFO:**

*** C-rate**

The charge and discharge current of a battery is measured in C-rate. Most portable batteries, are discharge with 1C. A discharge of 1C draws a current equal to the battery capacity. For example, a battery value of 1000mAh provides 1000mA for one hour if discharged at 1C. The same battery discharged at 0.5C provides 500mAfor two hours. At 2C, the same battery delivers 2000mA for 30 minutes. 1C is often referred to as a one-hour discharge; a 0.5 would be a two-hour, and a 0.1C a 10 hour discharge.

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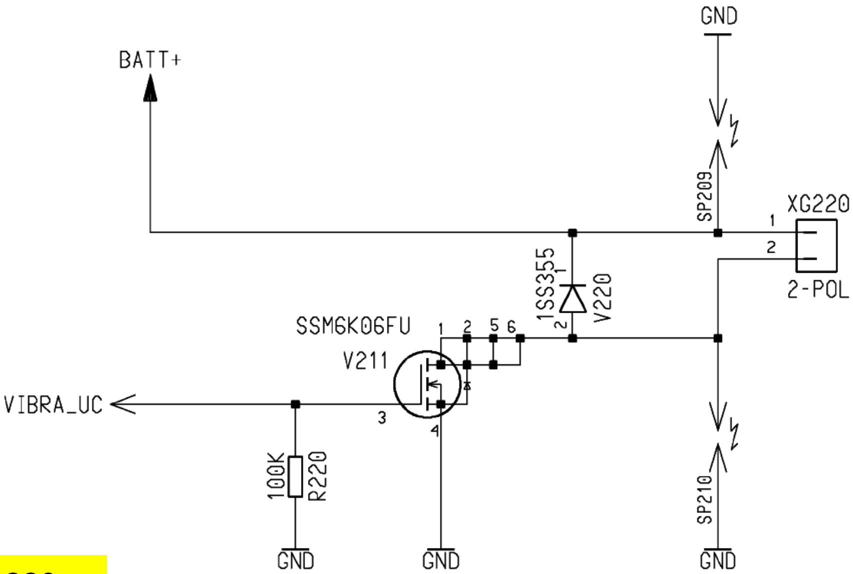
Restrictions

- A battery which has completely run down can not be re-charged quickly because the battery voltage is less than 3.0V and the logic which implements the charge control cannot be operated at this low voltage level. In this case the battery is recharged via trickle-charging. However, the charging symbol cannot be shown in the display because at this time logic supply voltages are not operating. The charging time for this trickle-charging (until the battery can be fast-charged from then on) is in the range of 1 hour. If, within this time, the battery voltage exceeds 3.2V, then the POWER SUPPLY ASIC switches on the mobile and charging continues in the Charge-Only Mode. In some circumstances it can happen that after trickle-charging and the usually initiated switch-on procedure of the mobile, the supply voltage collapses so much that the mobile phone switches off again. In this case trickle charging starts again with a now raised threshold voltage of 3.75V instead of 3.2V, at maximum for 20 minutes. The POWER SUPPLY ASIC will retry switching on the phone up to 3 times (within 60 minutes overall).
- Charging the battery will not be fully supported in case of using old accessory (generation '45' or earlier). It is not recommended to use any cables that adapt "old" to "new" Lumberg connector. Using such adapters with Marlin will have at least the following impact:
  1) half-sine wave chargers (e.g. P35 & home station) can not be used for trickle charging
  2) normal charging might be aborted before the battery is fully charged
  3) EMC compliance can not be guaranteed
- A phone with a fully charged LiIon battery will not be charged immediately after switch-on. Any input current would cause an increase of the battery voltage above the maximum permissible value. As soon as the battery has been discharged to a level of about 95% (due to current consumption while use), it will be re-charged in normal charging mode.
- The phone cannot be operated without a battery.
- The phone will be destroyed if the battery is inserted with reversed polarity:
  ⇒ design-wise it is impossible to wrongly pole the phone. This is prevented by mechanical means.
  ⇒ electrically, a correctly poled battery is presumed, i.e. correct polarity must be guaranteed by suitable QA measures at the supplier
- The mobile phone might be destroyed by connecting an unsuitable charger:
  ⇒ a charger voltage >15V can destroy resistances or capacitors
  ⇒ a charger voltage >20V can destroy the switch transistor of the charging circuit
  In case the transistor fails the ASIC will be destroyed. In the case of voltages lower than 15V and an improper current limitation the battery might be permanently damaged. A protection against grossly negligent use by the customer (e.g. direct connection of the charge contact to the electricity supply in a motor car) is not provided. Customer safety will not be affected by this restriction.

# 7 Interfaces

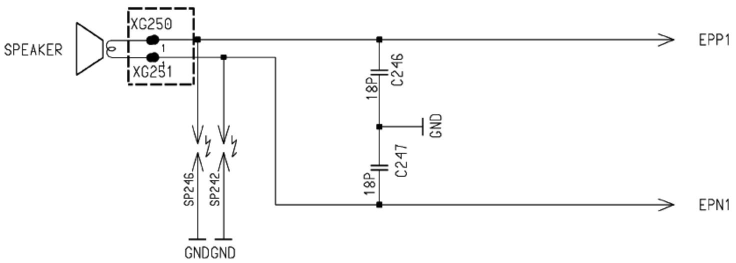
## 7.1 Vibra




**XG220**

| Pin | IN/OUT | Remarks |
|---|---|---|
| 1 | O | |
| 2 | O | The FET V211, switching this signal, is controlled via the EGOLD+ signal VIBRA_UC. |

## 7.2 Earpiece

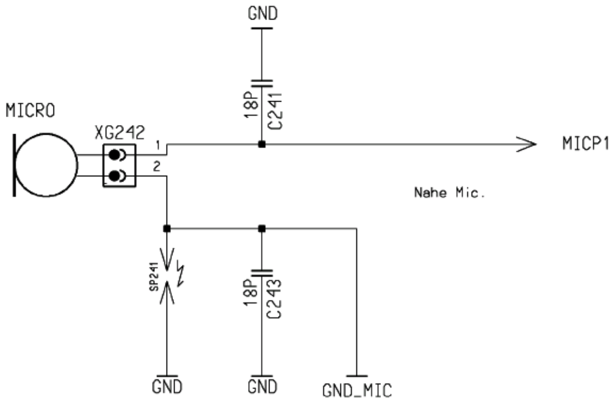



**XG250**

| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 1 | EPP1 | O | 1st connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. EPP1 builds together with EPN1 the differential output to drive the multifunctional “earpiece” (earpiece, ringer, handsfree function). |
| 2 | EPN1 | O | 2nd connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. |

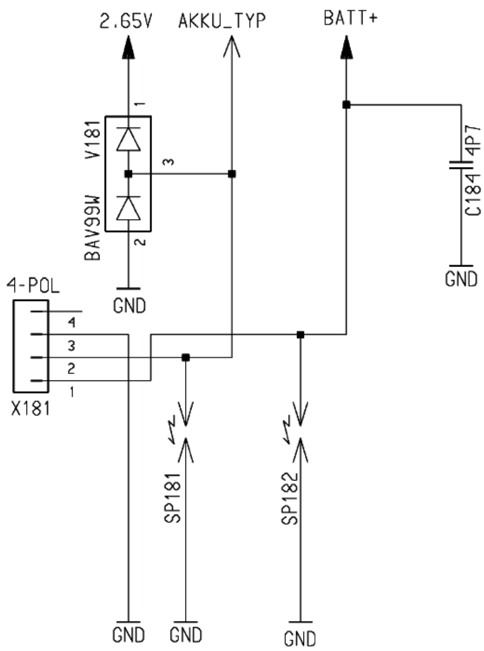
## 7.3 Microphone




**XG242**

| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 1 | MICP1 | O | Microphone power supply. The same line carries the low frequency speech signal. |
| 2 | MICN1 | I | Speech signal. The same line carries the microphone power supply. |
| 3 | GND_MIC | | |

## 7.4 Battery



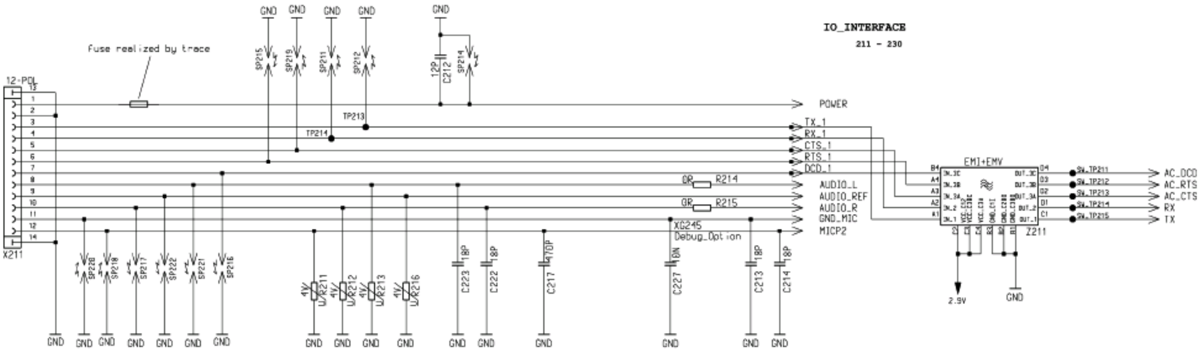

**XG181**

| Pin | Name | Level | Remarks |
|---|---|---|---|
| 1 | GND | - | Ground |
| 2 | AKKU_TYP | 0V...2.65V | Recognition of battery/supplier |
| 3 | BATT+ | 3 V... 4.5V | Positive battery pole |

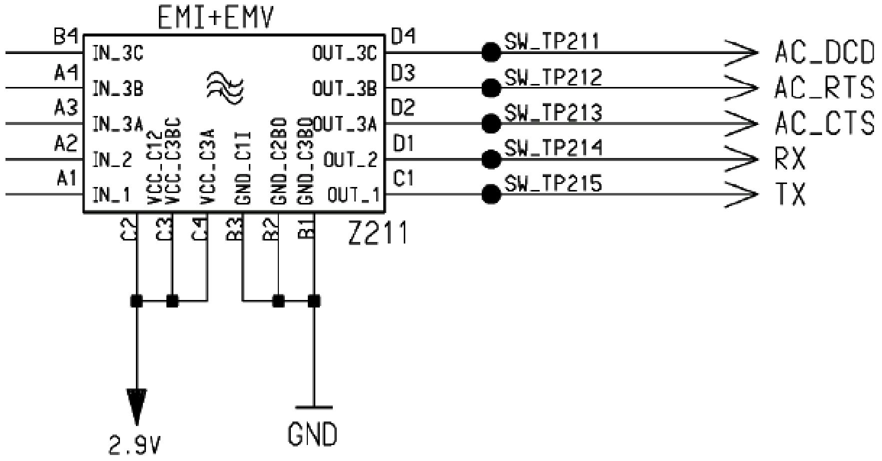
## 7.5 IO Connector with ESD protection

### 7.5.1 IO Connector – New Slim Lumberg



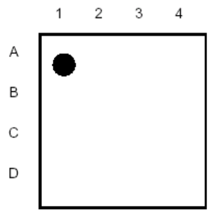

| Pin | Name | IN/OUT | Notes |
|---|---|---|---|
| 1 | POWER | I/O | POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories. |
| 2 | GND | | |
| 3 | TX | O | Serial interface |
| 4 | RX | I | serial interface |
| 5 | DATA/CTS | I/O | Data-line for accessory-bus<br>Use as CTS in data operation. |
| 6 | RTS | I/O | Use as RTS in data-operation. |
| 7 | CLK/DCD | I/O | Clock-line for accessory-bus.<br>Use as DTC in data-operation. |
| 8 | AUDIO_L | Analog O | driving ext. left speaker<br>With mono-headset Audio_L and Audio_R differential mode |
| 9 | AUDIO_REF | Analog O | mid-voltage<br>in stereo mode reference to<br>AUDIO_L and AUDIO_R in mono mode not used |
| 10 | AUDIO_R | Analog O | driving ext. right speaker With mono-headset Audio_L and Audio_R differential Signal |
| 11 | GND_MIC | Analog I | for ext. microphone |
| 12 | MICP2 | Analog I | External microphone |

### 7.5.2 ESD Protection with EMI filter




The Z211 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z211 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages up to 8 kV.

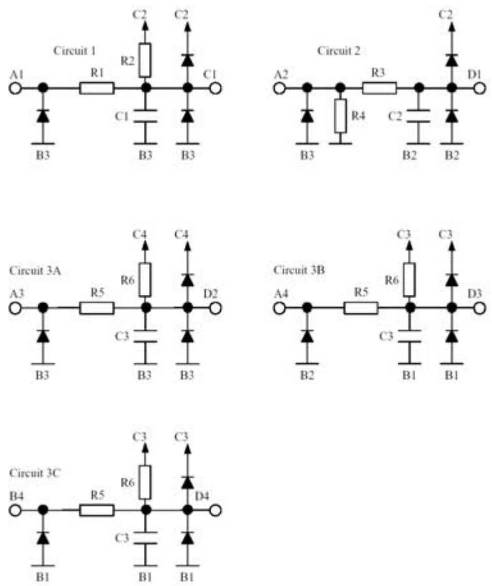
Pin configuration of the Z211



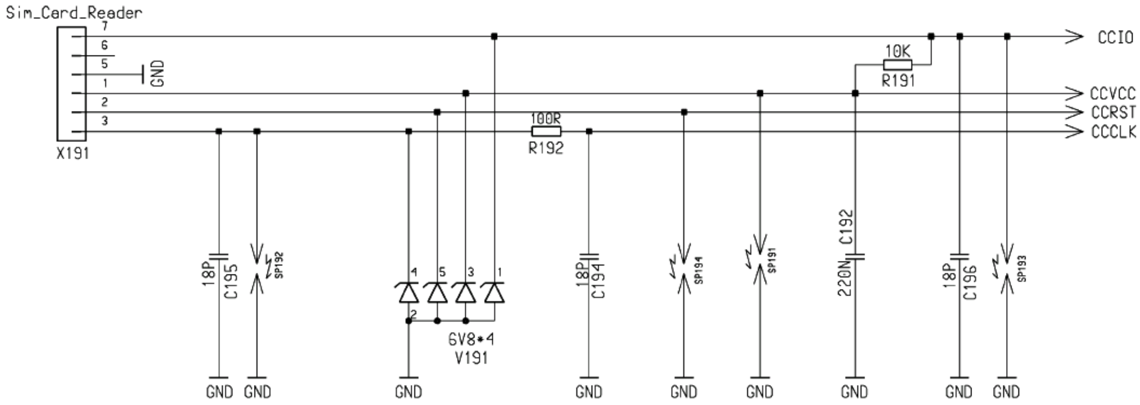
Top View (Bumps down)

| PIN | DESCRIPTION | PIN | DESCRIPTION |
|---|---|---|---|
| A1 | Input Circuit 1 | C1 | Output Circuit 1 |
| A2 | Input Circuit 2 | C2 | Vcc C1/C2 |
| A3 | Input Circuit 3A | C3 | Vcc C3B/C3C |
| A4 | Input Circuit 3B | C4 | Vcc C3A |
| B1 | GND C3Bo/C3Ci/C3Co | D1 | Output Circuit 2 |
| B2 | GND C2o/C3Bi | D2 | Output Circuit 3A |
| B3 | GND C1i/C1o/C2i/C3Ai/C3Ao | D3 | Output Circuit 3B |
| B4 | Input Circuit 3C | D4 | Output Circuit 3C |

Z211 Circuit Configuration

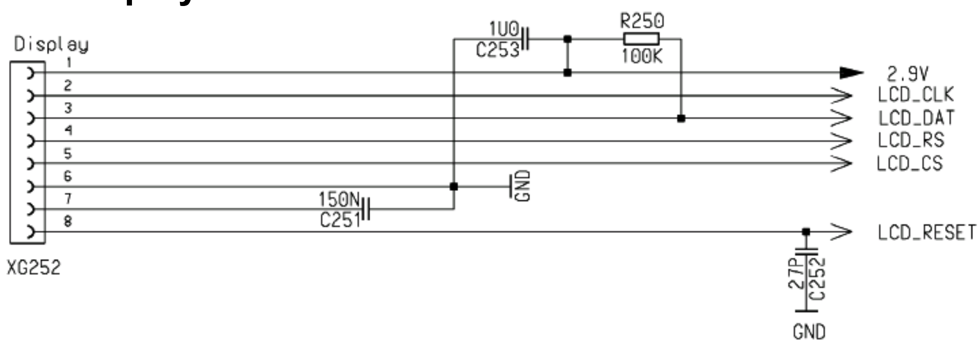


## 7.6 SIM




| Pin | Name | IN/OUT | Remarks |
|---|---|---|---|
| 3 | CCLK | O | Pulse for chipcard.<br>The chipcard is controlled directly from the EGOLD+. |
| 2 | CCRST | O | Reset for chipcard |
| 7 | CCIO | I<br>O | Data pin for chipcard;<br>10 kΩ pull up at the CCVCC pin |
| 1 | CCVCC | - | Switchable power supply for chipcard;<br>220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes. |

## 7.7 Display




| Pin | Name | Remarks |
|---|---|---|
| 1 | 2.9V | Power supply display controller |
| 2 | LCD_CLK | Clock |
| 3 | LCD_DAT | Data line |
| 4 | LCD_RS | Register select |
| 5 | LCD_CS | Chip select |
| 6 | GND | GND |
| 7 | VLCD | Power supply display |
| 8 | LCD_RESET | Reset |

# 8 Acoustic

The buzzer and the keypad clicks will be realized over the earpiece. At normal buzzer the signaling will realized with swelling tones. At the same time a maximum sound pressure level in the coupler of 135 +/- 5dB(A) is fixed.
The standard sounds will be generated by the EGOLD+, the advanced sounds will be generated via firmware running on the DSP.

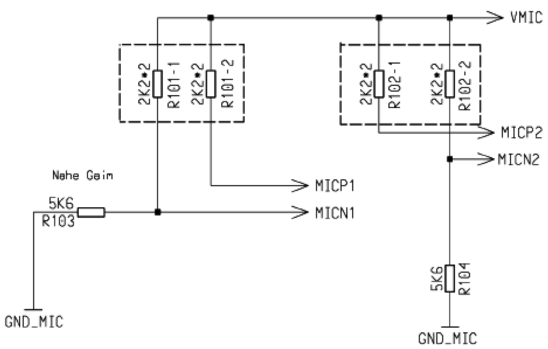
## 8.1 Microphone

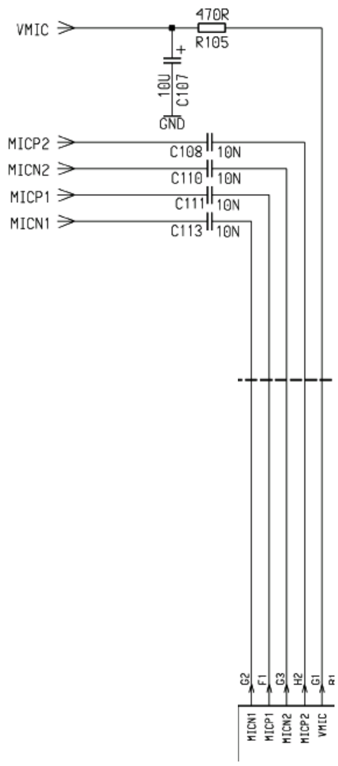
### 8.1.1 Mechanical

The microphone is built in the Mounting Frame Lower Part and is mechanically fixed with a rubber seal (gasket). The contact on the PCB is realised via spiral springs, which are integrated in the gasket. Because of usage of Unidirectional Microphone, the gasket has a front- and a back sound-inlet hole. The front sound-inlet is acoustically tighten connected with a sound-inlet at the rear-side of the mounting frame lower part. The back sound-inlet is acoustically tighten connected with a sound-inlet at the bottom-side of the mounting frame lower part. The gasket of the microphone has a asymmetrical shape in order to provide non-rotating, guaranteed covering of the sound-inlets of mounting frame lower part to the corresponding sound-inlets at microphone gasket.

### 8.1.2 Electrical

Both Microphones are directly connected to the EGOLD+.(Analog Interface G2, F1-G3, H2) via the signals MICN1, MICP1 (Internal Microphone )and MICN2, MICP2 (External Microphone/Headset). Power supply for the Microphone is VMIC (EGOLD+.(Analog Interface G1))



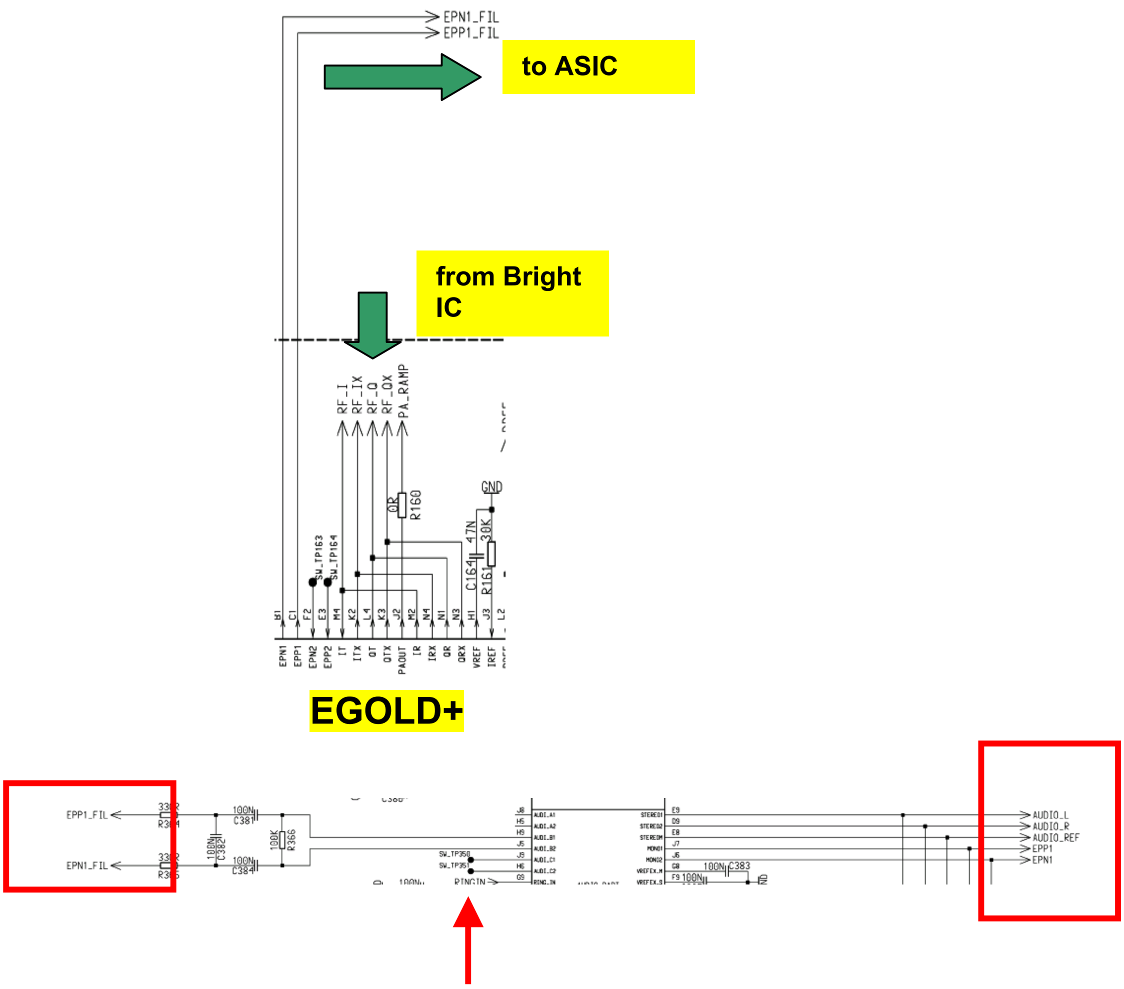
## 8.2 Earpiece/Loudspeaker

### 8.2.1 Mechanical

The speakermodule is designed to provide optimal performance for mobile handsfree and sound ringer. Plus independent from mobile leakage sound performance. Therefore speakermodule is a system that has a closed front volume with sound-outlets towards the ear of the user. Backvolume of Speakermodule is using the unused air between the antenna and the PCB. Backvolume is just used for resonance, there is no sound output from backvolume. The speakermodule is glued to the lightguide and contacted via two bending springs to the PCB. The lightguide itself is screwed with six screws via the PCB to the mounting frame lower part. Two of the six screws are located besides of the connection of speakermodule and lightguide. Therefore a good and reliable connection between speakermodule and PCB should be provided.

### 8.2.2 Electrical

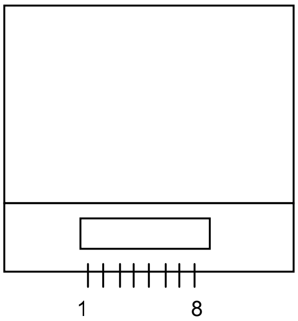
The internal and external Loudspeaker (Earpiece) is connected to the voiceband part of the EGOLD+ (Analog Interface B1, C1) via audio amplifier inside the ASIC (D361). Input EPN1_FIL - EPP1_FIL. Output for external loudspeaker AUDIO_L - AUDIO_R, for internal Loudspeaker EPP! – EPN1. The ringing tones are generated with the loudspeaker too. To activate the ringer, the signal RINGIN from the EGOLD+ (Miscellaneous,D16) is used



# 9 Display and Illumination

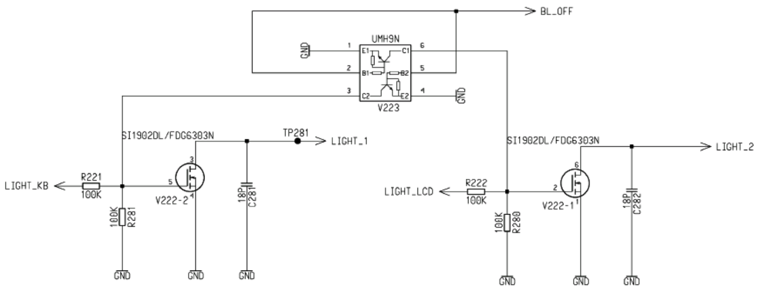
## 9.1 Display

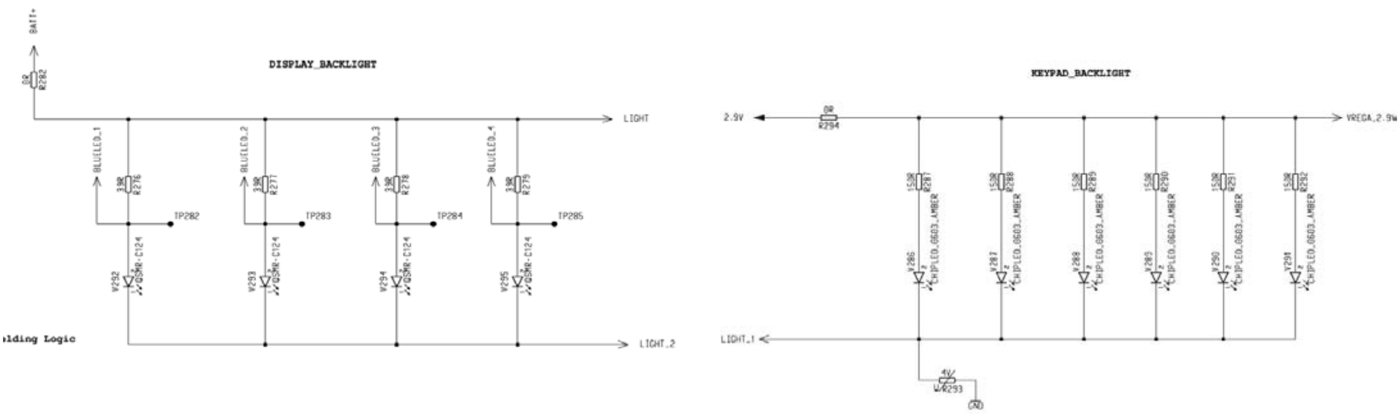
The display is provided with 2,65V from the ASIC (D361). The communication with the EGOLD+ by the LCD-Signals, directly connected to the EGOLD+




## 9.2 Illumination

The light is switched via switches inside the EGOLD+. With the signal LIGHT_KB (Miscellaneous T17) the illumination for the keyboard is controlled, with LIGHT_LCD. (GSM TDMA-Timer G15) the display backlight can be switched “on” and “off”. During the TX timeslot the light is deactivated via the signal BL_OFF (GSM TDAM-Timer G14)



# 10 Keyboard

The keyboard is connected via the lines KB0 – KB9 with the EGOLD+.
KB 7 is used for the ON/OFF switch. The lines KB0 – KB5 are used as output signals.
In the matrix KB6, KB8 and KB9 are used as input signals for the EGOLD+.